



Q67H2-AM

Rev : 1.0.

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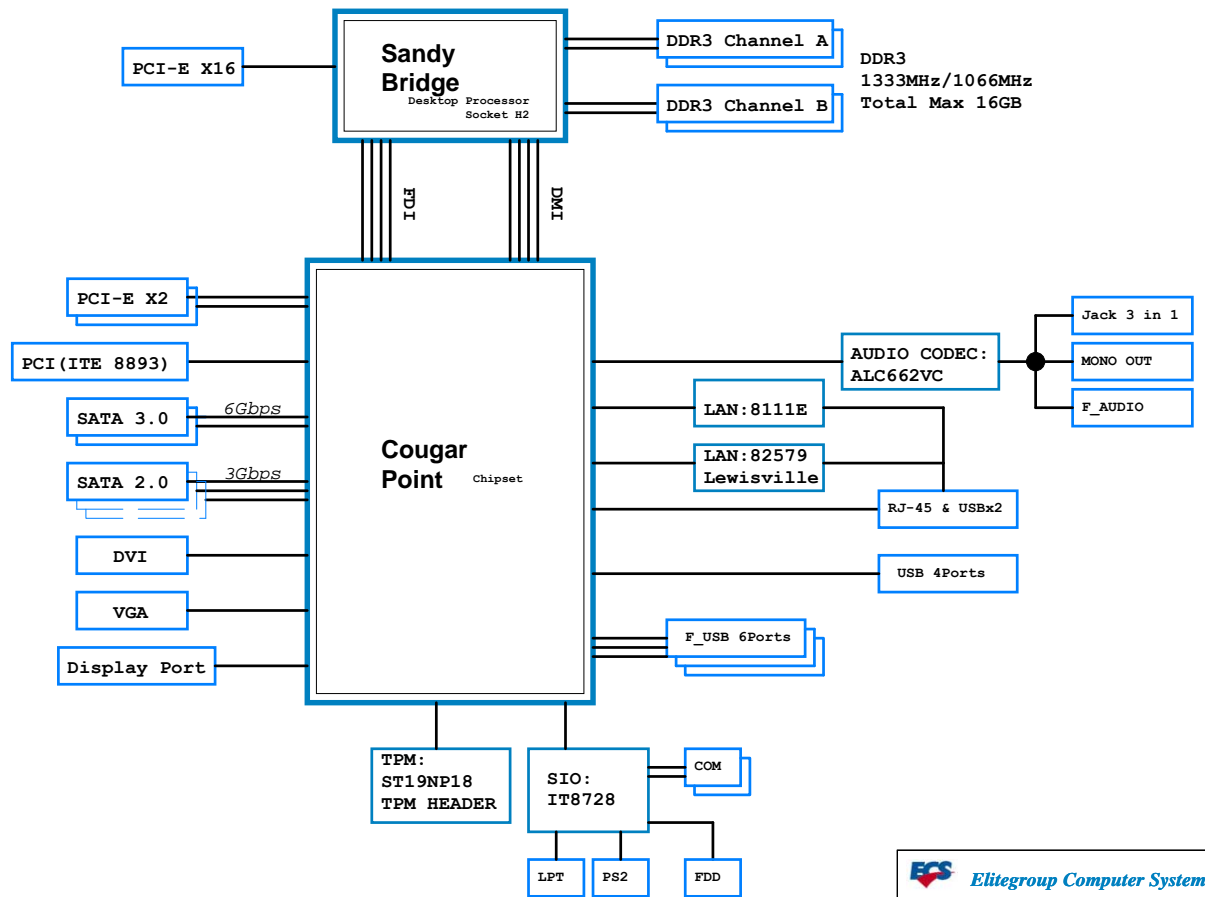
REVISION HISTORY:

Rev	Date	Notes
V.A	2010/04/19	Initial version
V.B	2010/09/13	
V.1.0	2010/09/30	

NOTE:
Design by
428971Sugar Bay and Bromolow-WS Platforms - Design Guide - Rev. 1.0,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

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Title			Cover Page
Rev	Document Number	Rev	
Custom	H67H2-AM/Q67H2-AM/Q65H2-AM	1.0.	
Date	Monday, November 22, 2010	Sheet	1 of 45

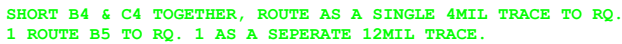


PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	OBR	GPI
GPIO12	3VSB	LAN_DISABLE_L	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO27	SB_3VSB	DEEP LANWAKEB	GPI
GPIO45	3VSB	SPI_WPSW	Native
GPIO59	3VSB	LAN_LED_D	Native
GPIO72	3VSB	SPI_WP0_L	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO16		SIO_BEEP	
GPIO22		SIO_LED1	
GPIO23		SIO_LED0	



9 M_DATA_A[0..63]	M_DATA_A[0..63]
9 M_DQS_A[P0..7]	M_DQS_A[P0..7]
9 M_DQS_A[N0..7]	M_DQS_A[N0..7]
9 M_MA_A[0..15]	M_MA_A[0..15]
9 M_BS_A[0..2]	M_BS_A[0..2]
9 M_CS_A[L0..3]	M_CS_A[L0..3]
9 M_CKE_A[0..3]	M_CKE_A[0..3]
9 M_ODT_A[0..3]	M_ODT_A[0..3]
9 M_CLK_A[P0..3]	M_CLK_A[P0..3]
9 M_CLK_A[N0..3]	M_CLK_A[N0..3]
9 M_WE_A_L	M_WE_A_L
9 M_CAS_A_L	M_CAS_A_L
9 M_RAS_A_L	M_RAS_A_L

DDR3 CH.A

9.10 DDR3_DRAMRST_L << DDR3_DRAMRST_L

10 M_DATA_B[0..63]	M_DATA_B[0..63]
10 M_DQS_B[P0..7]	M_DQS_B[P0..7]
10 M_DQS_B[N0..7]	M_DQS_B[N0..7]
10 M_MA_B[0..15]	M_MA_B[0..15]
10 M_BS_B[0..2]	M_BS_B[0..2]
10 M_CS_B[L0..3]	M_CS_B[L0..3]
10 M_CKE_B[0..3]	M_CKE_B[0..3]
10 M_ODT_B[0..3]	M_ODT_B[0..3]
10 M_CLK_B[P0..3]	M_CLK_B[P0..3]
10 M_CLK_B[N0..3]	M_CLK_B[N0..3]
10 M_WE_B_L	M_WE_B_L
10 M_CAS_B_L	M_CAS_B_L
10 M_RAS_B_L	M_RAS_B_L

DDR3 CH.B

M_DATA_A0 AJ3	SA_MA_0 AV27	M_MA_A0
M_DATA_A1 AJ2	SA_MA_1 AV24	M_MA_A1
M_DATA_A2 AL3	SA_MA_2 AW24	M_MA_A2
M_DATA_A3 AJ2	SA_MA_3 AV23	M_MA_A3
M_DATA_A4 AJ1	SA_MA_4 AT24	M_MA_A4
M_DATA_A5 AJ2	SA_MA_5 AT23	M_MA_A5
M_DATA_A6 AL1	SA_MA_6 AV22	M_MA_A6
M_DATA_A7 AN1	SA_MA_7 AT22	M_MA_A7
M_DATA_A8 AN4	SA_MA_8 AV22	M_MA_A8
M_DATA_A9 AN4	SA_MA_9 AT22	M_MA_A9
M_DATA_A10 AR4	SA_MA_10 AU21	M_MA_A10
M_DATA_A11 AN2	SA_MA_11 AT21	M_MA_A11
M_DATA_A12 AN2	SA_MA_12 AV22	M_MA_A12
M_DATA_A13 AR2	SA_MA_13 AU20	M_MA_A13
M_DATA_A14 AR2	SA_MA_14 AT20	M_MA_A14
M_DATA_A15 AV2	SA_MA_15	
M_DATA_A16 AV2		
M_DATA_A17 AV5		
M_DATA_A18 AW5		
M_DATA_A19 AW5		
M_DATA_A20 AU2		
M_DATA_A21 AU3		
M_DATA_A22 AU5		
M_DATA_A23 AV5		
M_DATA_A24 AU7		
M_DATA_A25 AU7		
M_DATA_A26 AU9		
M_DATA_A27 AU9		
M_DATA_A28 AV7		
M_DATA_A29 AV7		
M_DATA_A30 AW5		
M_DATA_A31 AY9		
M_DATA_A32 AU5		
M_DATA_A33 AU9		
M_DATA_A34 AU9		
M_DATA_A35 AU9		
M_DATA_A36 AU9		
M_DATA_A37 AU9		
M_DATA_A38 AU9		
M_DATA_A39 AU9		
M_DATA_A40 AR40		
M_DATA_A41 AR37		
M_DATA_A42 AN38		
M_DATA_A43 AN37		
M_DATA_A44 AR38		
M_DATA_A45 AR38		
M_DATA_A46 AN38		
M_DATA_A47 AN40		
M_DATA_A48 AL37		
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M_DATA_A55 AL40		
M_DATA_A56 AG40		
M_DATA_A57 AG37		
M_DATA_A58 AE38		
M_DATA_A59 AE37		
M_DATA_A60 AG38		
M_DATA_A61 AG38		
M_DATA_A62 AE39		
M_DATA_A63 AE40		
M_DQS_A_P0 AK3	SA_DQS_0	
M_DQS_A_P1 AV4	SA_DQS_1	
M_DQS_A_P2 AV4	SA_DQS_2	
M_DQS_A_P3 AV37	SA_DQS_3	
M_DQS_A_P4 AP36	SA_DQS_4	
M_DQS_A_P5 AK38	SA_DQS_5	
M_DQS_A_P6 AF38	SA_DQS_6	
M_DQS_A_P7 AF38	SA_DQS_7	
M_DQS_A_N0 AK2	SA_DQS#_0	
M_DQS_A_N1 AP22	SA_DQS#_1	
M_DQS_A_N2 AV42	SA_DQS#_2	
M_DQS_A_N3 AW38	SA_DQS#_3	
M_DQS_A_N4 AV36	SA_DQS#_4	
M_DQS_A_N5 AP36	SA_DQS#_5	
M_DQS_A_N6 AK39	SA_DQS#_6	
M_DQS_A_N7 AF39	SA_DQS#_7	

DDR_0

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SKT_H2_CRB

DDR3 CH.A

Pay Attention to This Part!

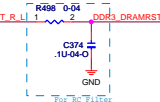
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M_DATA_B1 AG6	SB_DQ_1	
M_DATA_B2 AG6	SB_DQ_2	
M_DATA_B3 AG6	SB_DQ_3	
M_DATA_B4 AG6	SB_DQ_4	
M_DATA_B5 AG6	SB_DQ_5	
M_DATA_B6 AG6	SB_DQ_6	
M_DATA_B7 AG7	SB_DQ_7	
M_DATA_B8 AL7	SB_DQ_8	
M_DATA_B9 AM7	SB_DQ_9	
M_DATA_B10 AL7	SB_DQ_10	
M_DATA_B11 AL10	SB_DQ_11	
M_DATA_B12 AL10	SB_DQ_12	
M_DATA_B13 AL10	SB_DQ_13	
M_DATA_B14 AL3	SB_DQ_14	
M_DATA_B15 AL3	SB_DQ_15	
M_DATA_B16 AP7	SB_DQ_16	
M_DATA_B17 AP10	SB_DQ_17	
M_DATA_B18 AR10	SB_DQ_18	
M_DATA_B19 AR10	SB_DQ_19	
M_DATA_B20 AR6	SB_DQ_20	
M_DATA_B21 AR6	SB_DQ_21	
M_DATA_B22 AP5	SB_DQ_22	
M_DATA_B23 AR5	SB_DQ_23	
M_DATA_B24 AR5	SB_DQ_24	
M_DATA_B25 AM13	SB_DQ_25	
M_DATA_B26 AR13	SB_DQ_26	
M_DATA_B27 AR13	SB_DQ_27	
M_DATA_B28 AL12	SB_DQ_28	
M_DATA_B29 AL12	SB_DQ_29	
M_DATA_B30 AR12	SB_DQ_30	
M_DATA_B31 AR12	SB_DQ_31	
M_DATA_B32 AR6	SB_DQ_32	
M_DATA_B33 AR26	SB_DQ_33	
M_DATA_B34 AL29	SB_DQ_34	
M_DATA_B35 AL29	SB_DQ_35	
M_DATA_B36 AP26	SB_DQ_36	
M_DATA_B37 AP26	SB_DQ_37	
M_DATA_B38 AM29	SB_DQ_38	
M_DATA_B39 AP29	SB_DQ_39	
M_DATA_B40 AP30	SB_DQ_40	
M_DATA_B41 AP31	SB_DQ_41	
M_DATA_B42 AP32	SB_DQ_42	
M_DATA_B43 AR32	SB_DQ_43	
M_DATA_B44 AR32	SB_DQ_44	
M_DATA_B45 AR31	SB_DQ_45	
M_DATA_B46 AR31	SB_DQ_46	
M_DATA_B47 AR34	SB_DQ_47	
M_DATA_B48 AM31	SB_DQ_48	
M_DATA_B49 AL36	SB_DQ_49	
M_DATA_B50 AL32	SB_DQ_50	
M_DATA_B51 AL32	SB_DQ_51	
M_DATA_B52 AM34	SB_DQ_52	
M_DATA_B53 AL31	SB_DQ_53	
M_DATA_B54 AL34	SB_DQ_54	
M_DATA_B55 AL35	SB_DQ_55	
M_DATA_B56 AL34	SB_DQ_56	
M_DATA_B57 AE34	SB_DQ_57	
M_DATA_B58 AE35	SB_DQ_58	
M_DATA_B59 AL35	SB_DQ_59	
M_DATA_B60 AP33	SB_DQ_60	
M_DATA_B61 AL34	SB_DQ_61	
M_DATA_B62 AP33	SB_DQ_62	
M_DATA_B63 AF35	SB_DQ_63	
M_DQS_B_P0 AH7	SB_DQS_0	
M_DQS_B_P1 AR8	SB_DQS_1	
M_DQS_B_P2 AR8	SB_DQS_2	
M_DQS_B_P3 AN28	SB_DQS_3	
M_DQS_B_P4 AP38	SB_DQS_4	
M_DQS_B_P5 AL37	SB_DQS_5	
M_DQS_B_P6 AG35	SB_DQS_6	
M_DQS_B_P7 AG35	SB_DQS_7	
M_DQS_B_N0 AH6	SB_DQS#_0	
M_DQS_B_N1 AL6	SB_DQS#_1	
M_DQS_B_N2 AP38	SB_DQS#_2	
M_DQS_B_N3 AN28	SB_DQS#_3	
M_DQS_B_N4 AN28	SB_DQS#_4	
M_DQS_B_N5 AM33	SB_DQS#_5	
M_DQS_B_N6 AM33	SB_DQS#_6	
M_DQS_B_N7 AG34	SB_DQS#_7	

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SKT_H2_CRB

DDR3 CH.B

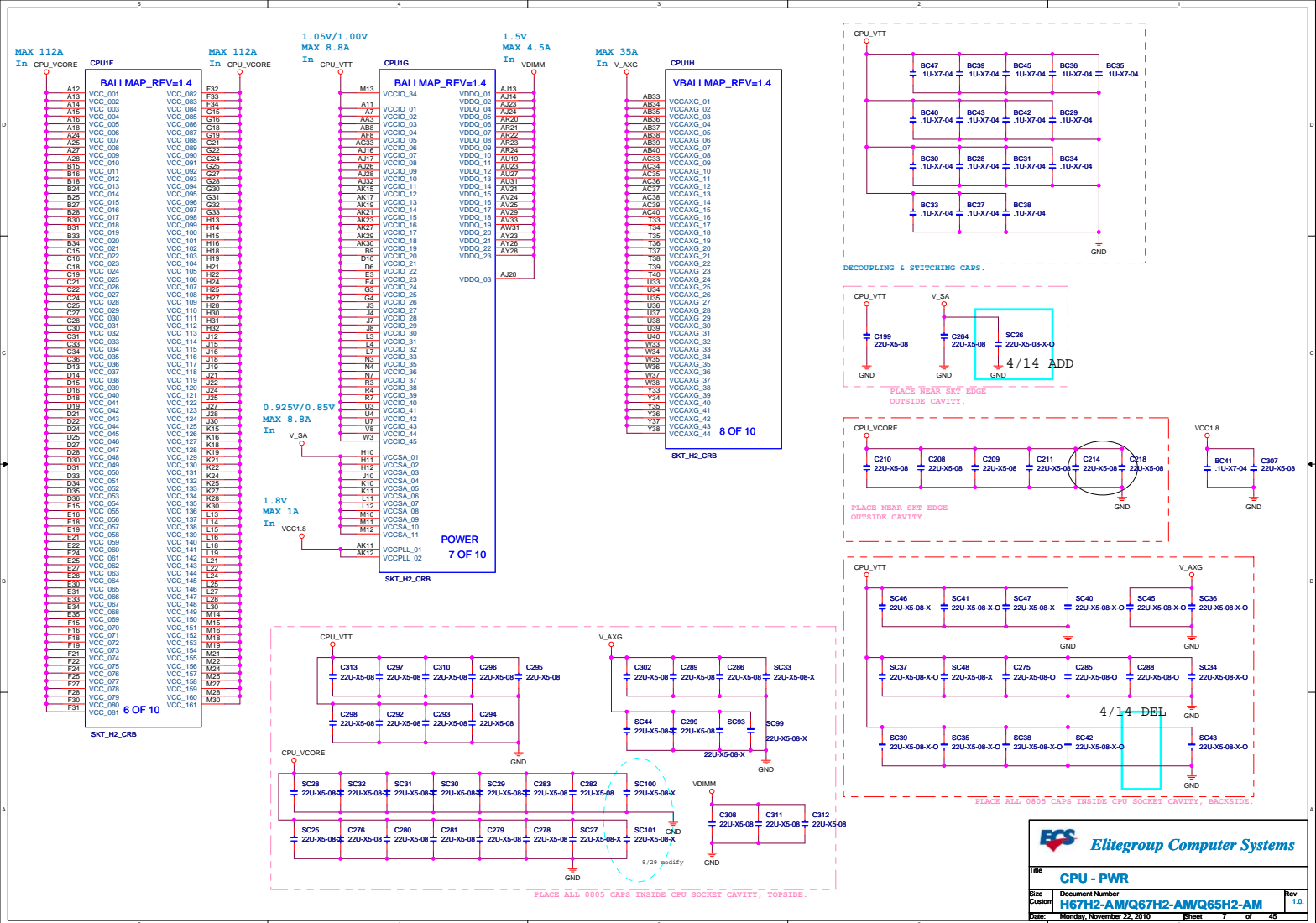


Desktop doesn't support ECC

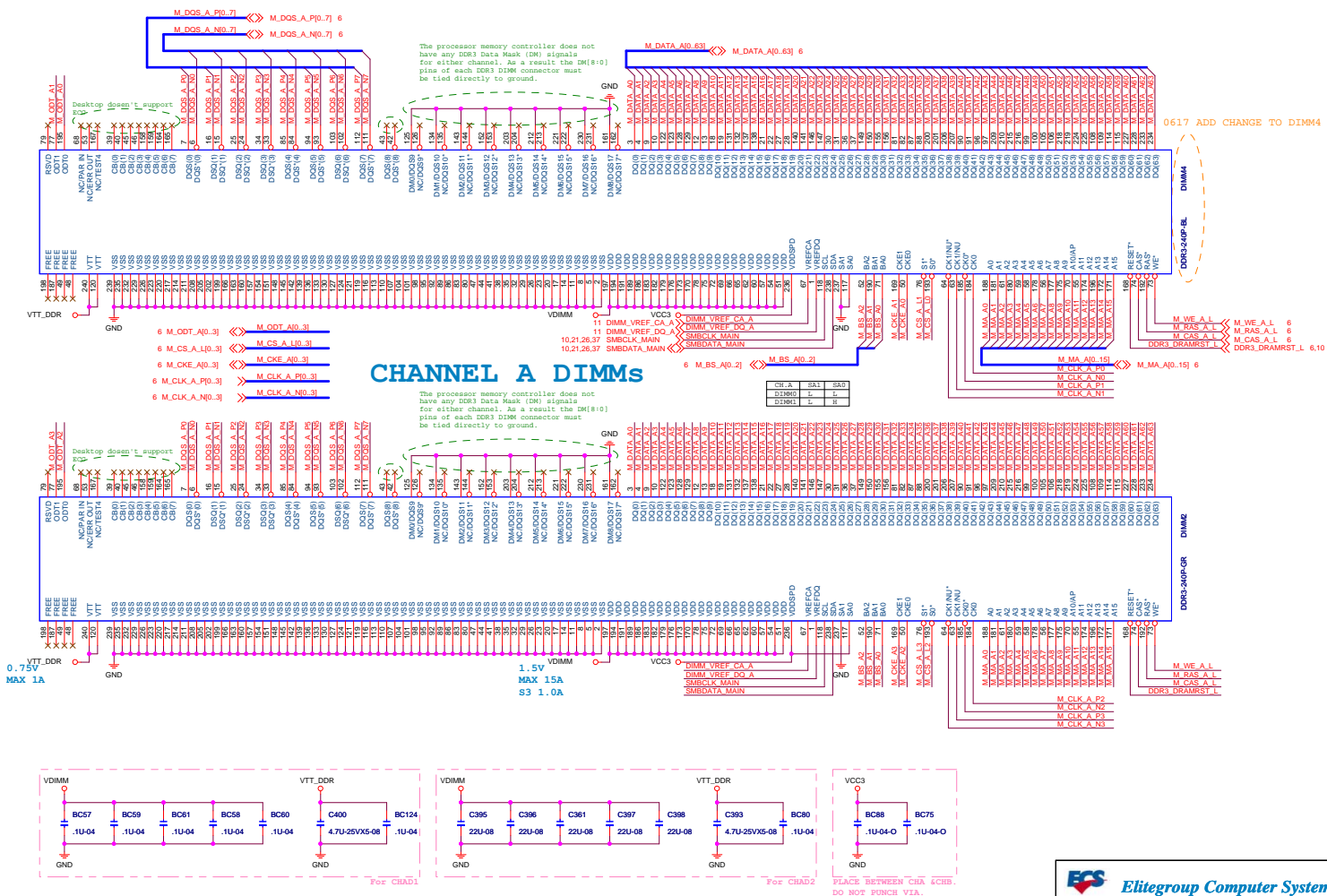
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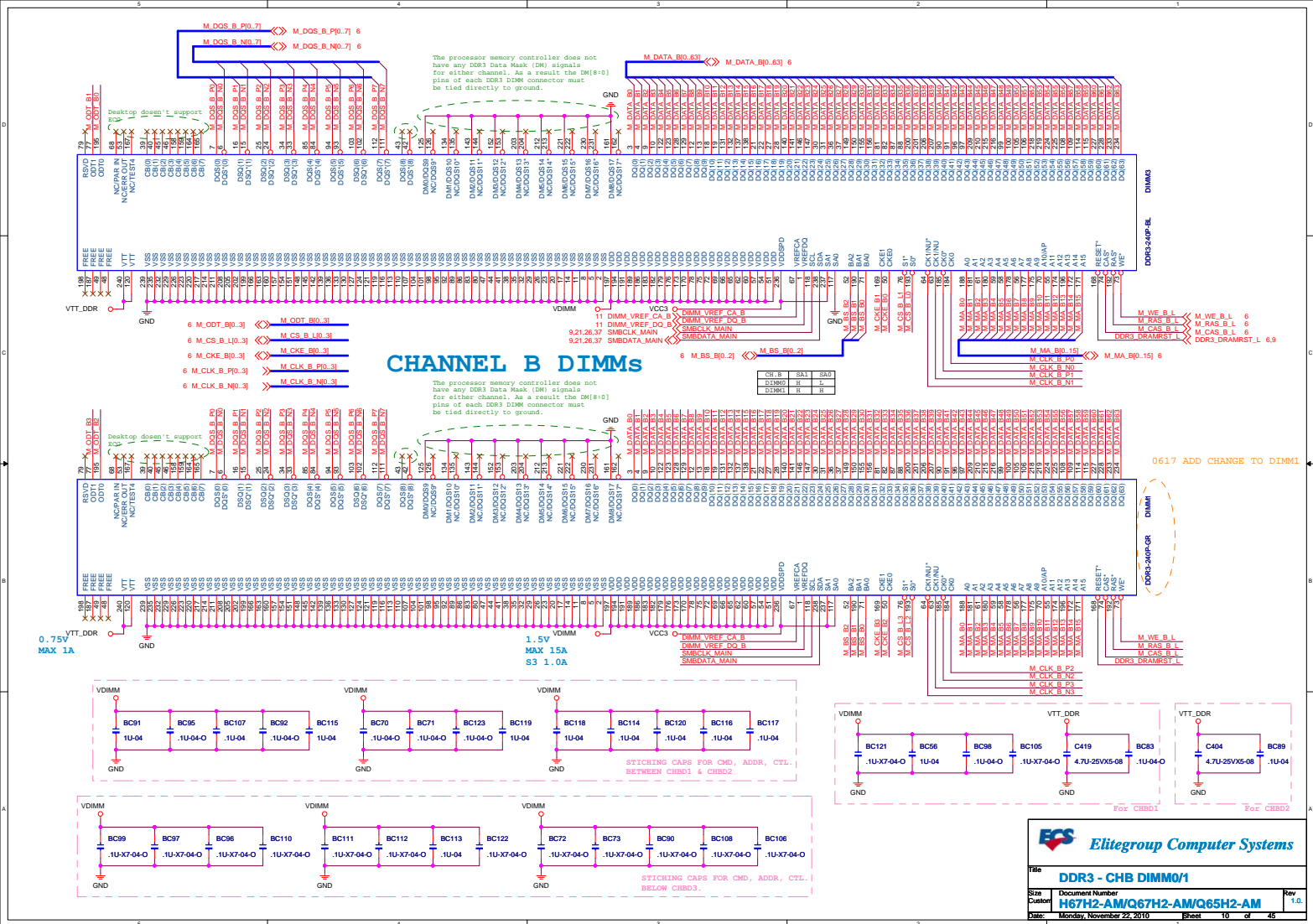
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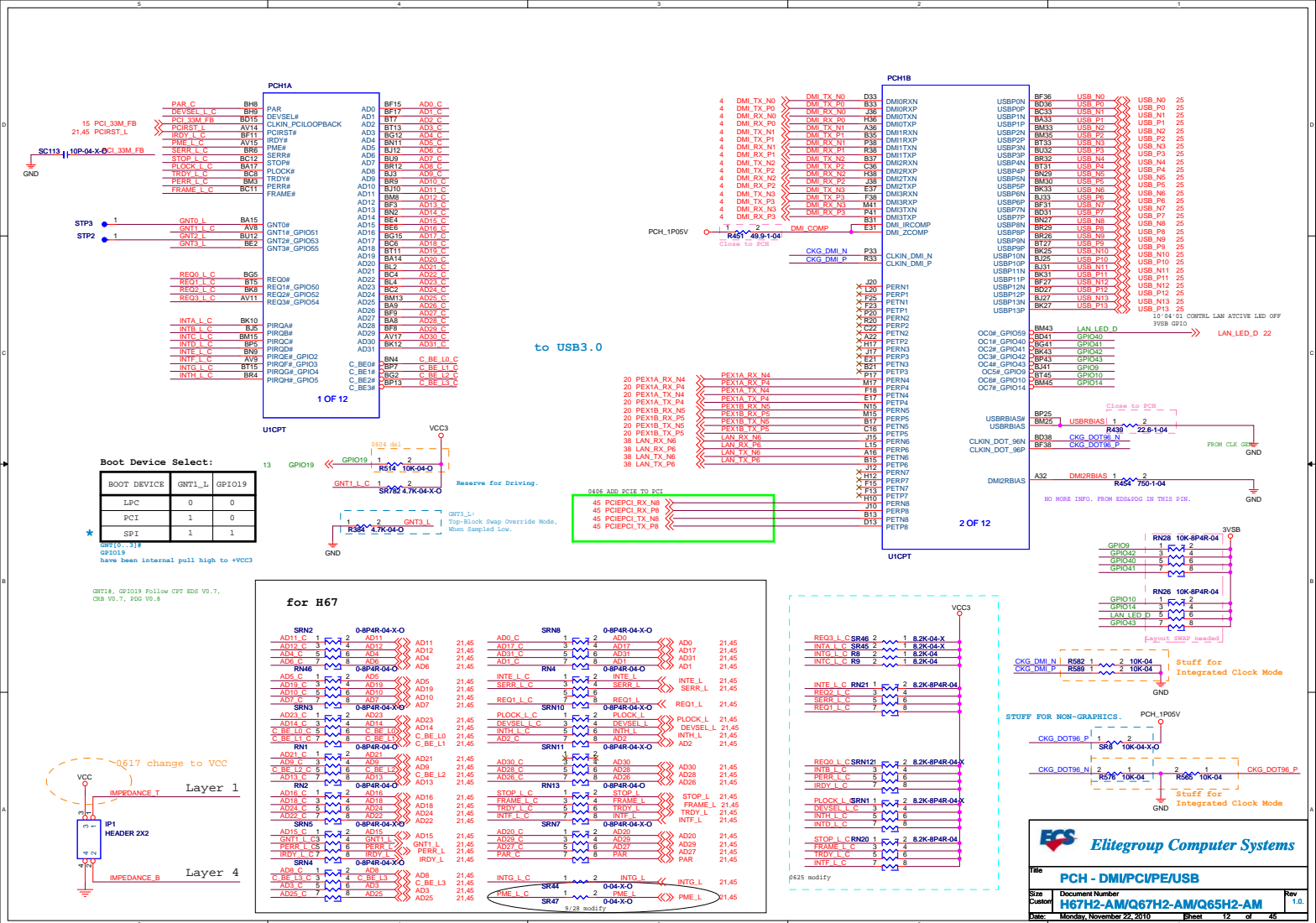
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CPU - DDR3		
Size	Document Number	Rev
Customer	H67H2-AM/Q67H2-AM/Q65H2-AM	1.0
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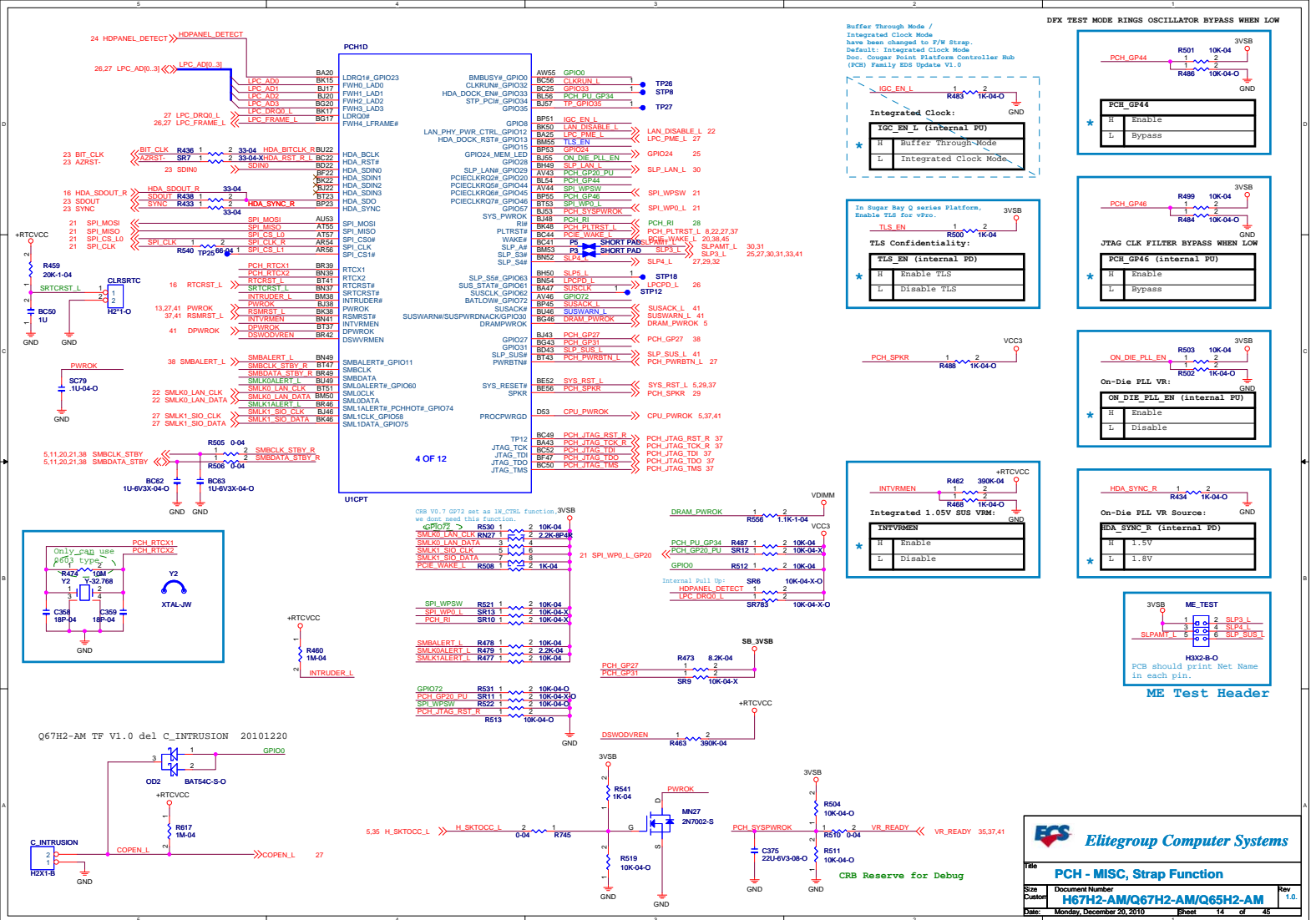
CPU11			CPU12		
BALLMAP_REV1.4			BALLMAP_REV1.4		
A17	VSS_001	AM27	AV11	VSS_161	G8
A25	VSS_002	AM28	AV12	VSS_162	H17
A26	VSS_003	AM29	AV13	VSS_163	H2
A28	VSS_004	AM30	AV14	VSS_164	H20
AX33	VSS_005	AM31	AV15	VSS_165	H23
AX35	VSS_006	AM32	AV16	VSS_166	H26
AX36	VSS_007	AM33	AV17	VSS_167	H29
AX37	VSS_008	AM34	AV18	VSS_168	H33
AX38	VSS_009	AM35	AV19	VSS_169	H35
AX39	VSS_010	AM36	AV20	VSS_170	H37
AX40	VSS_011	AM37	AV21	VSS_171	H39
AX41	VSS_012	AM38	AV22	VSS_172	H42
AX42	VSS_013	AM39	AV23	VSS_173	H45
AX43	VSS_014	AM40	AV24	VSS_174	H48
AX44	VSS_015	AM41	AV25	VSS_175	H51
AX45	VSS_016	AM42	AV26	VSS_176	H54
AX46	VSS_017	AM43	AV27	VSS_177	H57
AX47	VSS_018	AM44	AV28	VSS_178	H60
AX48	VSS_019	AM45	AV29	VSS_179	H63
AX49	VSS_020	AM46	AV30	VSS_180	H66
AX50	VSS_021	AM47	AV31	VSS_181	H69
AX51	VSS_022	AM48	AV32	VSS_182	H72
AX52	VSS_023	AM49	AV33	VSS_183	H75
AX53	VSS_024	AM50	AV34	VSS_184	H78
AX54	VSS_025	AM51	AV35	VSS_185	H81
AX55	VSS_026	AM52	AV36	VSS_186	H84
AX56	VSS_027	AM53	AV37	VSS_187	H87
AX57	VSS_028	AM54	AV38	VSS_188	H90
AX58	VSS_029	AM55	AV39	VSS_189	H93
AX59	VSS_030	AM56	AV40	VSS_190	H96
AX60	VSS_031	AM57	AV41	VSS_191	H99
AX61	VSS_032	AM58	AV42	VSS_192	H102
AX62	VSS_033	AM59	AV43	VSS_193	H105
AX63	VSS_034	AM60	AV44	VSS_194	H108
AX64	VSS_035	AM61	AV45	VSS_195	H111
AX65	VSS_036	AM62	AV46	VSS_196	H114
AX66	VSS_037	AM63	AV47	VSS_197	H117
AX67	VSS_038	AM64	AV48	VSS_198	H120
AX68	VSS_039	AM65	AV49	VSS_199	H123
AX69	VSS_040	AM66	AV50	VSS_200	H126
AX70	VSS_041	AM67	AV51	VSS_201	H129
AX71	VSS_042	AM68	AV52	VSS_202	H132
AX72	VSS_043	AM69	AV53	VSS_203	H135
AX73	VSS_044	AM70	AV54	VSS_204	H138
AX74	VSS_045	AM71	AV55	VSS_205	H141
AX75	VSS_046	AM72	AV56	VSS_206	H144
AX76	VSS_047	AM73	AV57	VSS_207	H147
AX77	VSS_048	AM74	AV58	VSS_208	H150
AX78	VSS_049	AM75	AV59	VSS_209	H153
AX79	VSS_050	AM76	AV60	VSS_210	H156
AX80	VSS_051	AM77	AV61	VSS_211	H159
AX81	VSS_052	AM78	AV62	VSS_212	H162
AX82	VSS_053	AM79	AV63	VSS_213	H165
AX83	VSS_054	AM80	AV64	VSS_214	H168
AX84	VSS_055	AM81	AV65	VSS_215	H171
AX85	VSS_056	AM82	AV66	VSS_216	H174
AX86	VSS_057	AM83	AV67	VSS_217	H177
AX87	VSS_058	AM84	AV68	VSS_218	H180
AX88	VSS_059	AM85	AV69	VSS_219	H183
AX89	VSS_060	AM86	AV70	VSS_220	H186
AX90	VSS_061	AM87	AV71	VSS_221	H189
AX91	VSS_062	AM88	AV72	VSS_222	H192
AX92	VSS_063	AM89	AV73	VSS_223	H195
AX93	VSS_064	AM90	AV74	VSS_224	H198
AX94	VSS_065	AM91	AV75	VSS_225	H201
AX95	VSS_066	AM92	AV76	VSS_226	H204
AX96	VSS_067	AM93	AV77	VSS_227	H207
AX97	VSS_068	AM94	AV78	VSS_228	H210
AX98	VSS_069	AM95	AV79	VSS_229	H213
AX99	VSS_070	AM96	AV80	VSS_230	H216
AX100	VSS_071	AM97	AV81	VSS_231	H219
AX101	VSS_072	AM98	AV82	VSS_232	H222
AX102	VSS_073	AM99	AV83	VSS_233	H225
AX103	VSS_074	AM100	AV84	VSS_234	H228
AX104	VSS_075	AM101	AV85	VSS_235	H231
AX105	VSS_076	AM102	AV86	VSS_236	H234
AX106	VSS_077	AM103	AV87	VSS_237	H237
AX107	VSS_078	AM104	AV88	VSS_238	H240
AX108	VSS_079	AM105	AV89	VSS_239	H243
AX109	VSS_080	AM106	AV90	VSS_240	H246
AX110	VSS_081	AM107	AV91	VSS_241	H249
AX111	VSS_082	AM108	AV92	VSS_242	H252
AX112	VSS_083	AM109	AV93	VSS_243	H255
AX113	VSS_084	AM110	AV94	VSS_244	H258
AX114	VSS_085	AM111	AV95	VSS_245	H261
AX115	VSS_086	AM112	AV96	VSS_246	H264
AX116	VSS_087	AM113	AV97	VSS_247	H267
AX117	VSS_088	AM114	AV98	VSS_248	H270
AX118	VSS_089	AM115	AV99	VSS_249	H273
AX119	VSS_090	AM116	AV100	VSS_250	H276
AX120	VSS_091	AM117	AV101	VSS_251	H279
AX121	VSS_092	AM118	AV102	VSS_252	H282
AX122	VSS_093	AM119	AV103	VSS_253	H285
AX123	VSS_094	AM120	AV104	VSS_254	H288
AX124	VSS_095	AM121	AV105	VSS_255	H291
AX125	VSS_096	AM122	AV106	VSS_256	H294
AX126	VSS_097	AM123	AV107	VSS_257	H297
AX127	VSS_098	AM124	AV108	VSS_258	H300
AX128	VSS_099	AM125	AV109	VSS_259	H303
AX129	VSS_100	AM126	AV110	VSS_260	H306
AX130	VSS_101	AM127	AV111	VSS_261	H309
AX131	VSS_102	AM128	AV112	VSS_262	H312
AX132	VSS_103	AM129	AV113	VSS_263	H315
AX133	VSS_104	AM130	AV114	VSS_264	H318
AX134	VSS_105	AM131	AV115	VSS_265	H321
AX135	VSS_106	AM132	AV116	VSS_266	H324
AX136	VSS_107	AM133	AV117	VSS_267	H327
AX137	VSS_108	AM134	AV118	VSS_268	H330
AX138	VSS_109	AM135	AV119	VSS_269	H333
AX139	VSS_110	AM136	AV120	VSS_270	H336
AX140	VSS_111	AM137	AV121	VSS_271	H339
AX141	VSS_112	AM138	AV122	VSS_272	H342
AX142	VSS_113	AM139	AV123	VSS_273	H345
AX143	VSS_114	AM140	AV124	VSS_274	H348
AX144	VSS_115	AM141	AV125	VSS_275	H351
AX145	VSS_116	AM142	AV126	VSS_276	H354
AX146	VSS_117	AM143	AV127	VSS_277	H357
AX147	VSS_118	AM144	AV128	VSS_278	H360
AX148	VSS_119	AM145	AV129	VSS_279	H363
AX149	VSS_120	AM146	AV130	VSS_280	H366
AX150	VSS_121	AM147	AV131	VSS_281	H369
AX151	VSS_122	AM148	AV132	VSS_282	H372
AX152	VSS_123	AM149	AV133	VSS_283	H375
AX153	VSS_124	AM150	AV134	VSS_284	H378
AX154	VSS_125	AM151	AV135	VSS_285	H381
AX155	VSS_126	AM152	AV136	VSS_286	H384
AX156	VSS_127	AM153	AV137	VSS_287	H387
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AX159	VSS_130	AM156	AV140	VSS_290	H396
AX160	VSS_131	AM157	AV141	VSS_291	H399
AX161	VSS_132	AM158	AV142	VSS_292	H402
AX162	VSS_133	AM159	AV143	VSS_293	H405
AX163	VSS_134	AM160	AV144	VSS_294	H408
AX164	VSS_135	AM161	AV145	VSS_295	H411
AX165	VSS_136	AM162	AV146	VSS_296	H414
AX166	VSS_137	AM163	AV147	VSS_297	H417
AX167	VSS_138	AM164	AV148	VSS_298	H420
AX168	VSS_139	AM165	AV149	VSS_299	H423
AX169	VSS_140	AM166	AV150	VSS_300	H426
AX170	VSS_141	AM167	AV151	VSS_301	H429
AX171	VSS_142	AM168	AV152	VSS_302	H432
AX172	VSS_143	AM169	AV153	VSS_303	H435
AX173	VSS_144	AM170	AV154	VSS_304	H438
AX174	VSS_145	AM171	AV155	VSS_305	H441
AX175	VSS_146	AM172	AV156	VSS_306	H444
AX176	VSS_147	AM173	AV157	VSS_307	H447
AX177	VSS_148	AM174	AV158	VSS_308	H450
AX178	VSS_149	AM175	AV159	VSS_309	H453
AX179	VSS_150	AM176	AV160	VSS_310	H456
AX180	VSS_151	AM177	AV161	VSS_311	H459
AX181	VSS_152	AM178	AV162	VSS_312	H462
AX182	VSS_153	AM179	AV163	VSS_313	H465
AX183	VSS_154	AM180	AV164	VSS_314	H468
AX184	VSS_155	AM181	AV165	VSS_315	H471
AX185	VSS_156	AM182	AV166	VSS_316	H474
AX186	VSS_157	AM183	AV167	VSS_317	H477
AX187	VSS_158	AM184	AV168	VSS_318	H480
AX188	VSS_159	AM185	AV169	VSS_319	H483
AX189	VSS_160	AM186	AV170	VSS_320	H486
AX190	VSS_161	AM187	AV171	VSS_321	H489
AX191	VSS_162	AM188	AV172	VSS_322	H492
AX192	VSS_163	AM189	AV173	VSS_323	H495
AX193	VSS_164	AM190	AV174	VSS_324	H498
AX194	VSS_165	AM191	AV175	VSS_325	H501
AX195	VSS_166	AM192	AV176	VSS_326	H504
AX196	VSS_167	AM193	AV177	VSS_327	H507
AX197	VSS_168	AM194	AV178	VSS_328	H510
AX198	VSS_169	AM195	AV179	VSS_329	H513
AX199	VSS_170	AM196	AV180	VSS_330	H516
AX200	VSS_171	AM197	AV181	VSS_331	H519
AX201	VSS_172	AM198	AV182	VSS_332	H522
AX202	VSS_173	AM199	AV183	VSS_333	H525
AX203	VSS_174	AM200	AV184	VSS_334	H528
AX204	VSS_175	AM201	AV185	VSS_335	H531
AX205	VSS_176	AM202	AV186	VSS_336	H534
AX206	VSS_177	AM203	AV187	VSS_337	H537
AX207	VSS_178	AM204	AV188	VSS_338	H540
AX208	VSS_179	AM205	AV189	VSS_339	H543
AX209	VSS_180	AM206	AV190	VSS_340	H546
AX210	VSS_181	AM207	AV191	VSS_341	H549
AX211	VSS_182	AM208	AV192	VSS_342	H552
AX212	VSS_183	AM209	AV193	VSS_343	H555
AX213	VSS_184	AM210	AV194	VSS_344	H558
AX214	VSS_185	AM211	AV195	VSS_345	H561
AX215	VSS_186	AM212	AV196	VSS_346	H564
AX216	VSS_187	AM213	AV197	VSS_347	H567
AX217	VSS_188	AM214	AV198	VSS_348	H570
AX218	VSS_189	AM215	AV199	VSS_349	H573
AX219	VSS_190	AM216	AV200	VSS_350	H576
AX220	VSS_191	AM217	AV201	VSS_351	H579
AX221	VSS_192	AM218	AV202	VSS_352	H582
AX222	VSS_193	AM219	AV203	VSS_353	H585
AX223	VSS_194	AM220	AV204	VSS_354	H588
AX224	VSS_195	AM221	AV205	VSS_355	H591
AX225	VSS_196	AM222	AV206	VSS_356	H594
AX226	VSS_197	AM223	AV207	VSS_357	H597
AX227	VSS_198	AM224	AV208	VSS_358	H600
AX228	VSS_199	AM225	AV209	VSS_359	H603
AX229	VSS_200	AM226	AV210	VSS_360	H606
AX230	VSS_201	AM227	AV211	VSS_361	H609
AX231	VSS_202	AM228	AV212	VSS_362	H612
AX232	VSS_203	AM229	AV213	VSS_363	H615
AX233	VSS_204	AM230	AV214	VSS_364	H618
AX234	VSS_205	AM231	AV215	VSS_365	H621
AX235	VSS_206	AM232	AV216	VSS_366	H624
AX236	VSS_207	AM233	AV217	VSS_367	H627
AX237	VSS_208	AM234	AV218	VSS_368	H

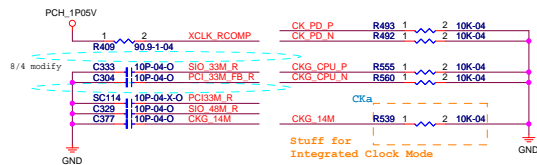






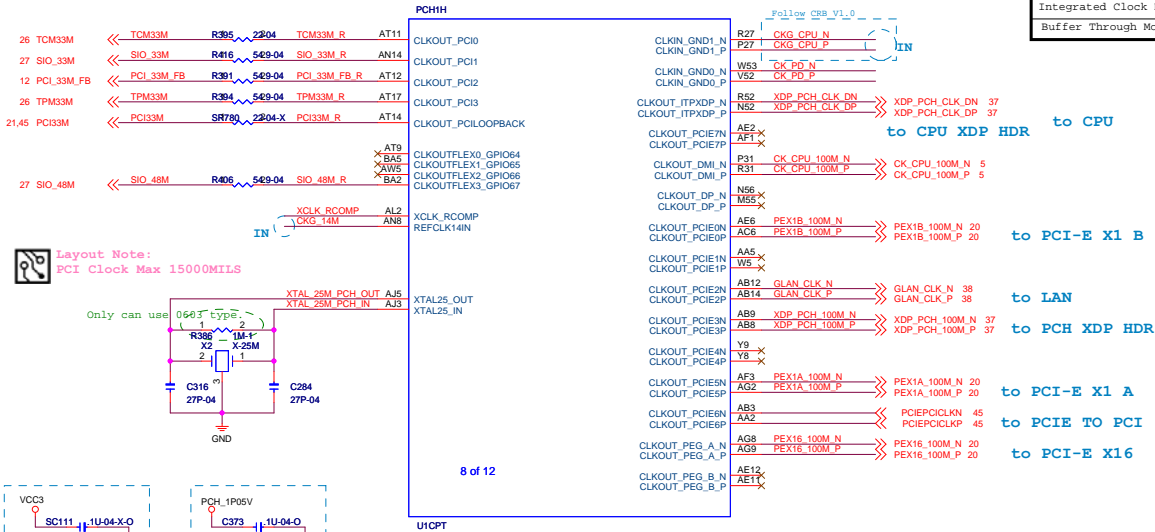
REQ0_L_C





10'03'24

Clock Mode	CLK GEN. Seligo SLG421 Circuit..	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X

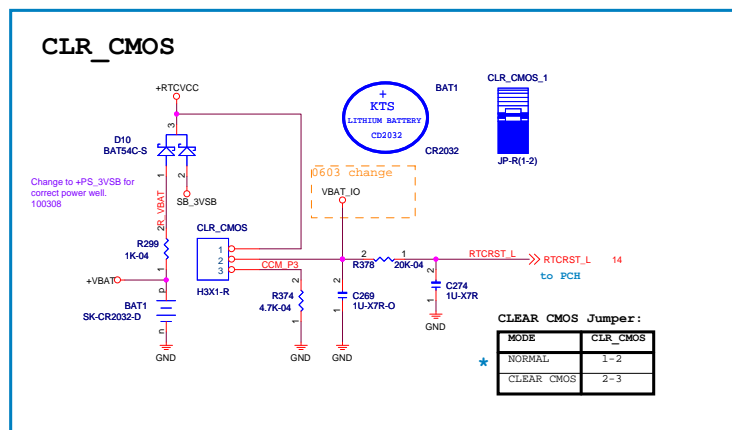
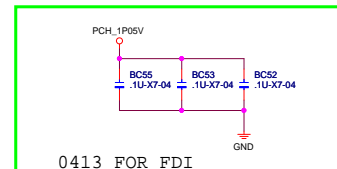
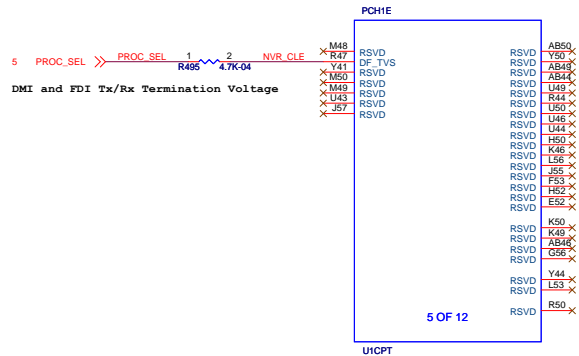


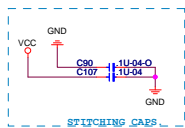
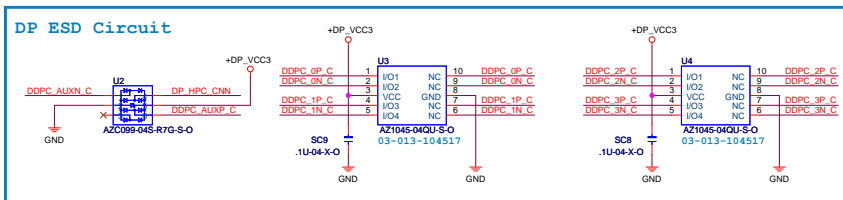
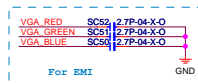
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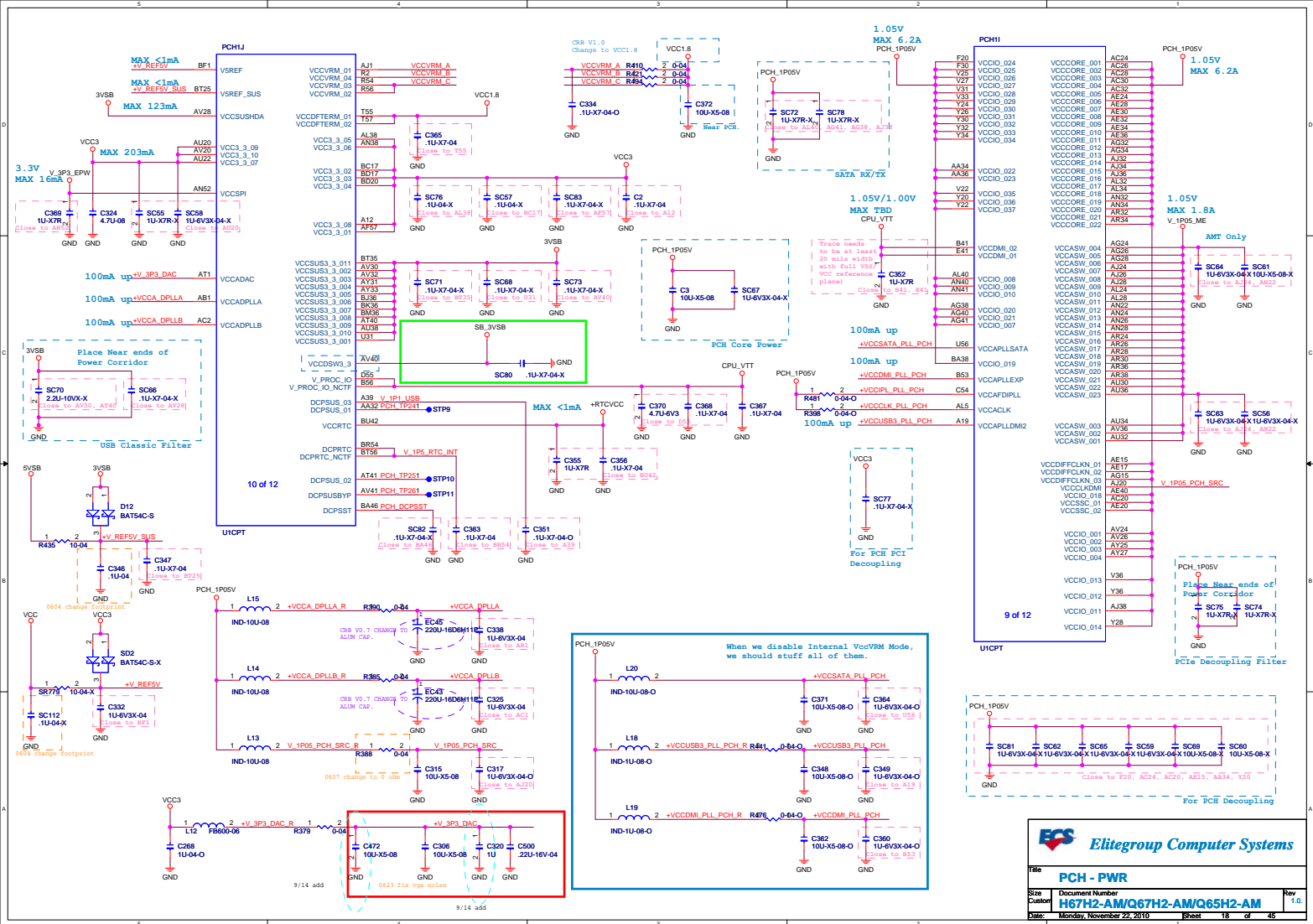
Title: **PCH - CLK IO, CKG - SLG421**

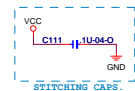
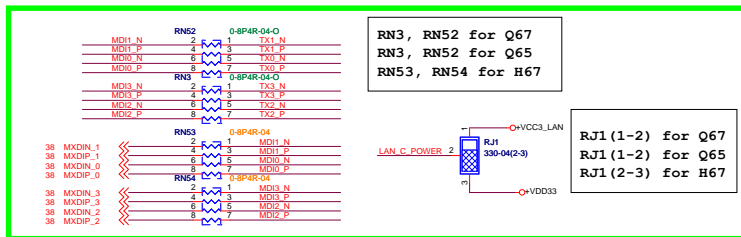
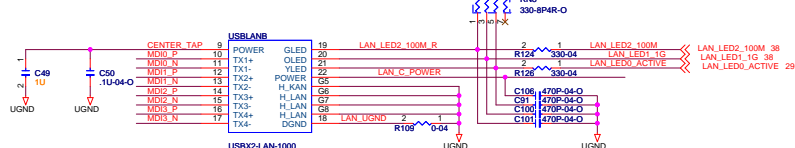
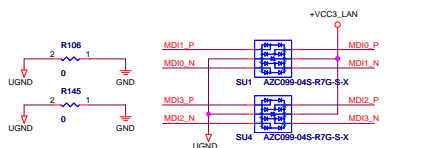
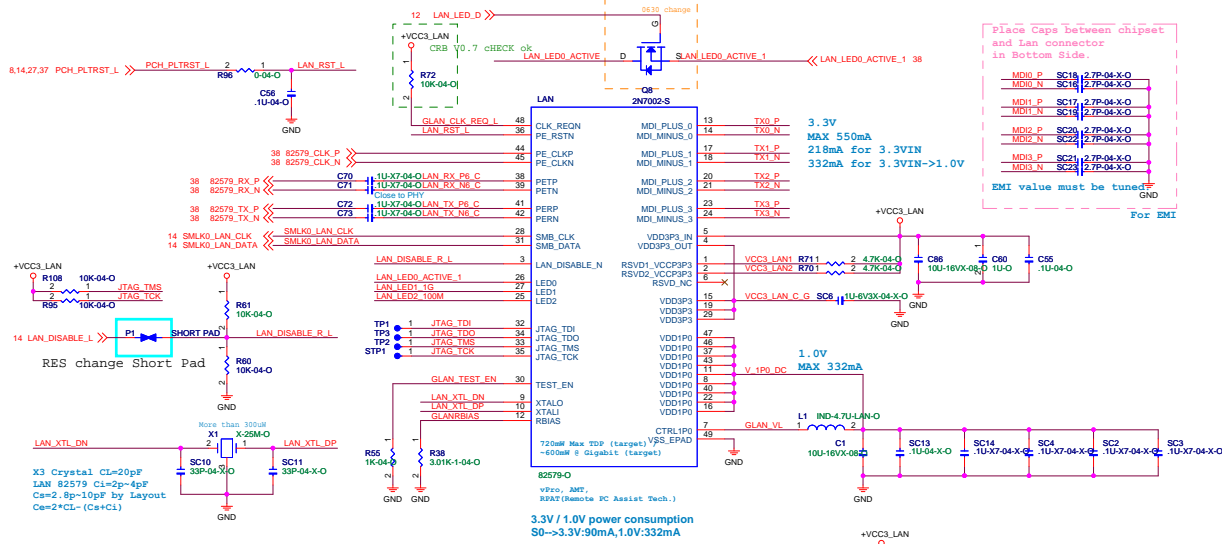
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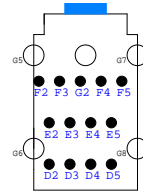
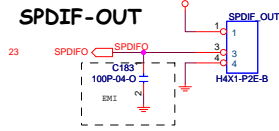
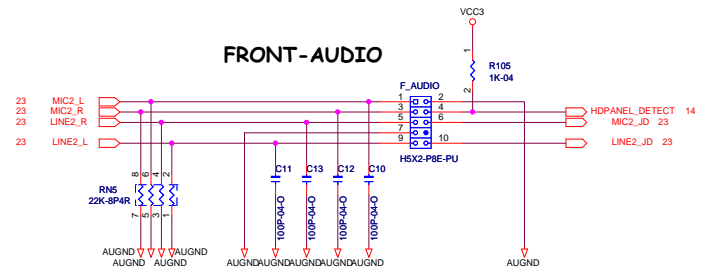
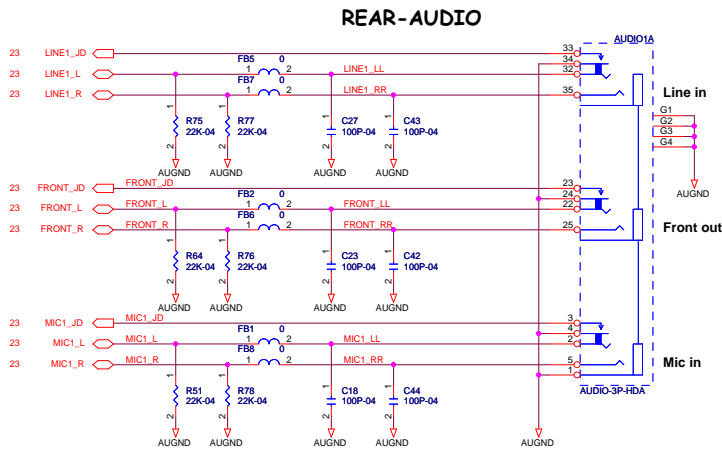
Date: **Monday, November 22, 2010** Sheet: **15** of **45**



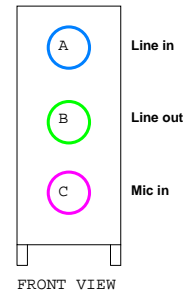









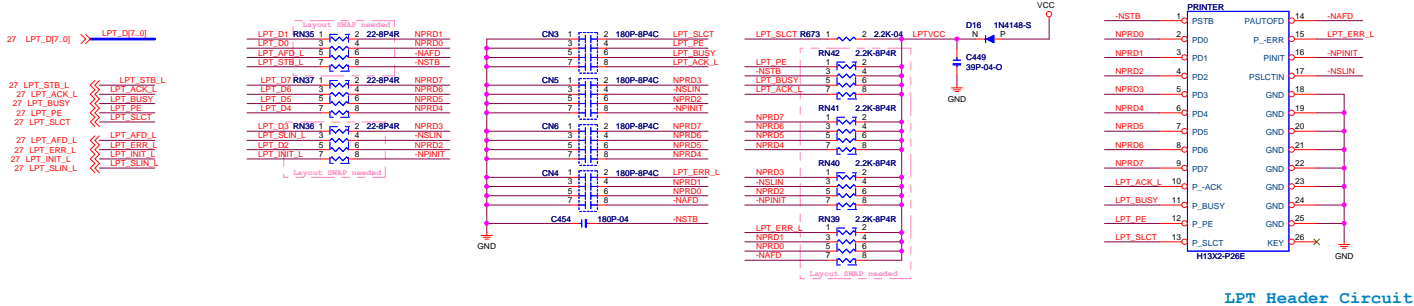
TOP VIEW



FRONT VIEW

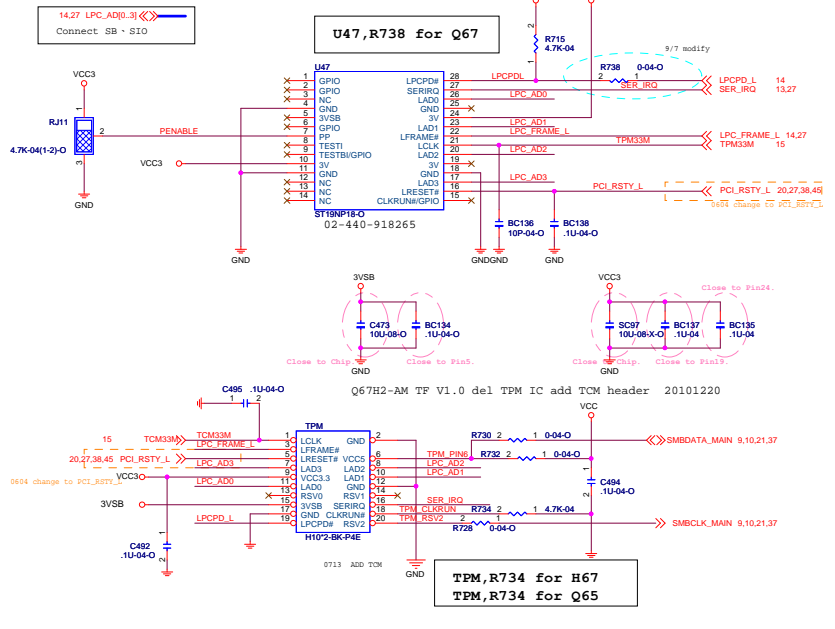
AUDIO ALC662 (PANEL)			
File			
Size	Document Number	Rev	
B	H67H2-AM/Q67H2-AM/Q65H2-AM	1.0	
Date:	Monday, November 22, 2010	Sheet	24 of 45

 Elitegroup Computer Systems			
File USB - PWR/CONN/HDR			
Size	Document Number		Rev
Customer	H67H2-AM/Q67H2-AM/Q65H2-AM		1.0
Date	Monday, November 22, 2010		Sheet 25 of 45

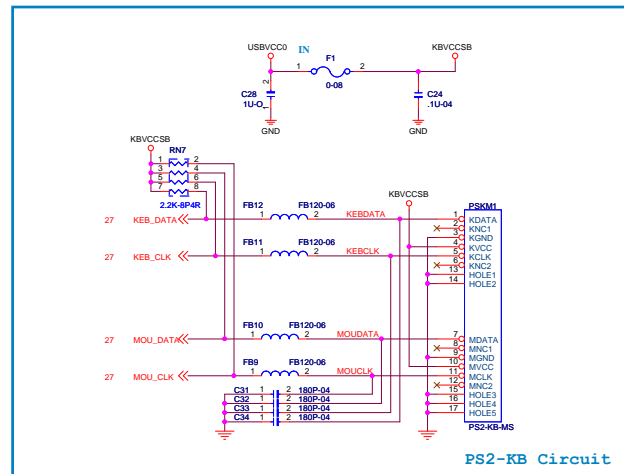


LPT Header Circuit

TPM CHIP/Header Circuit



TPM, R734 for H67
TPM, R734 for Q65



PS2-KB Circuit

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File: **TPM, PS/2, LPT**

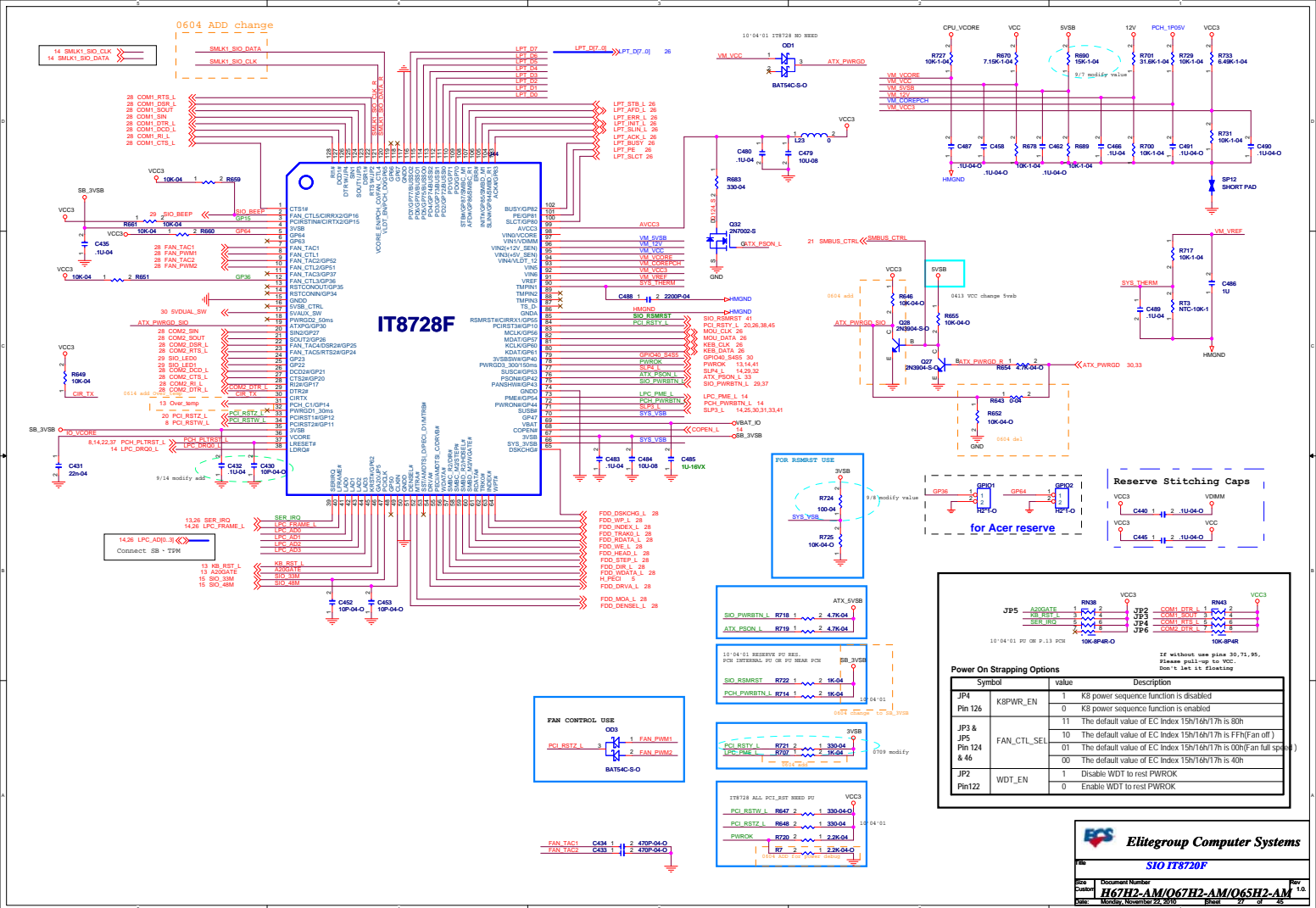
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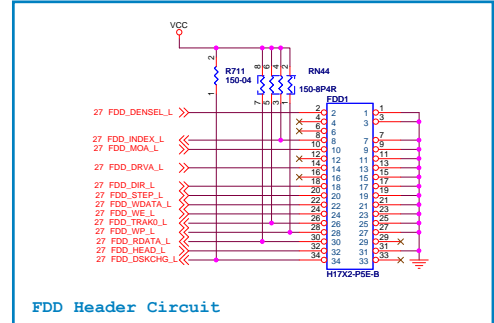
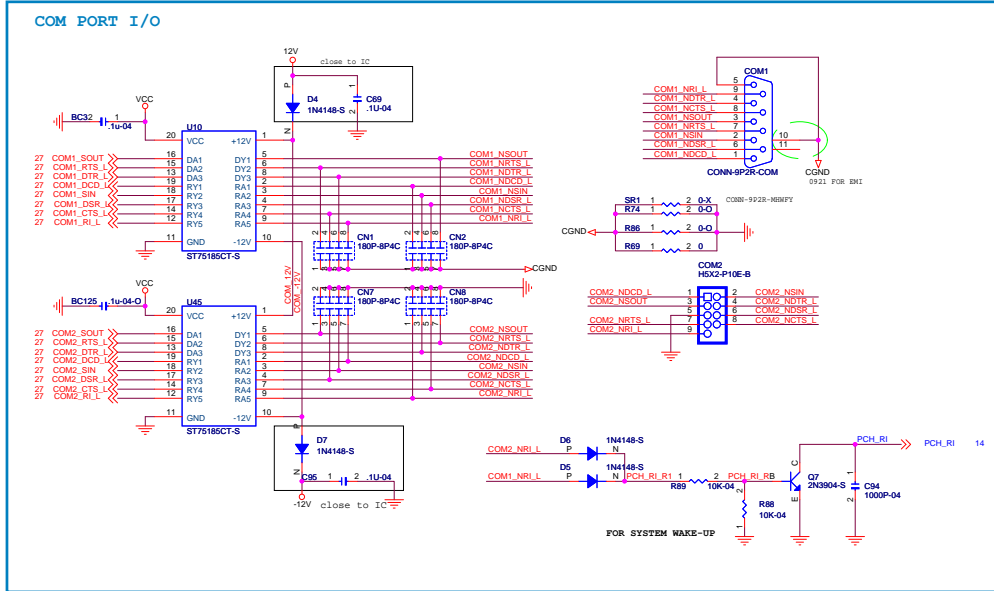
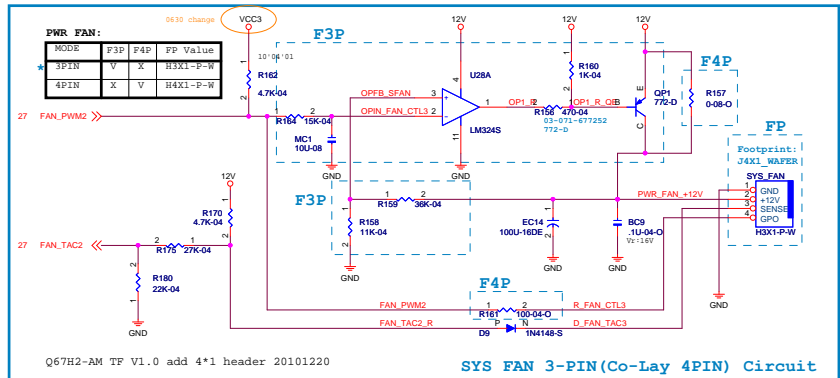
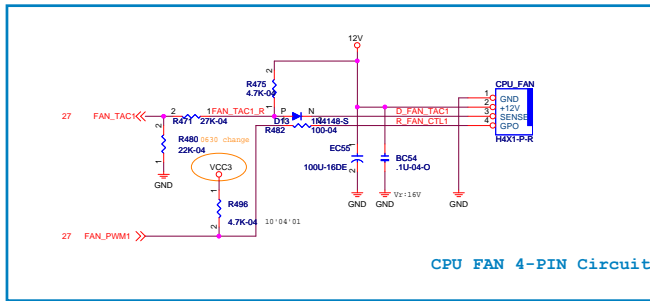
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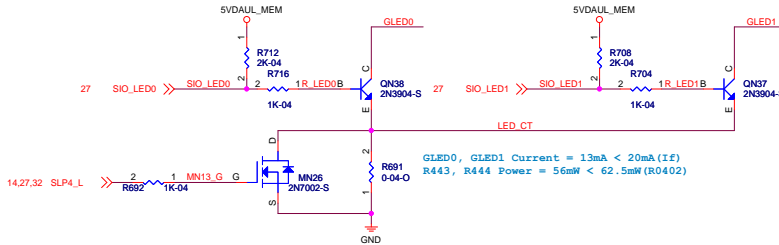
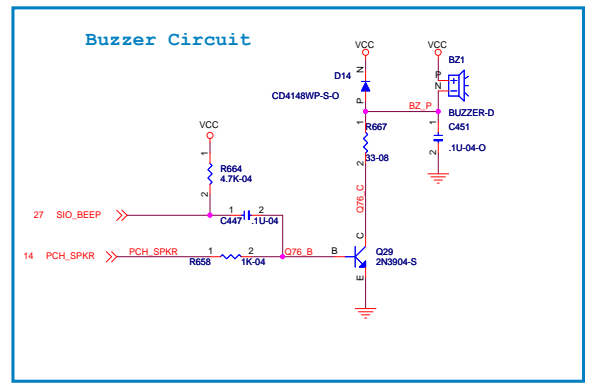
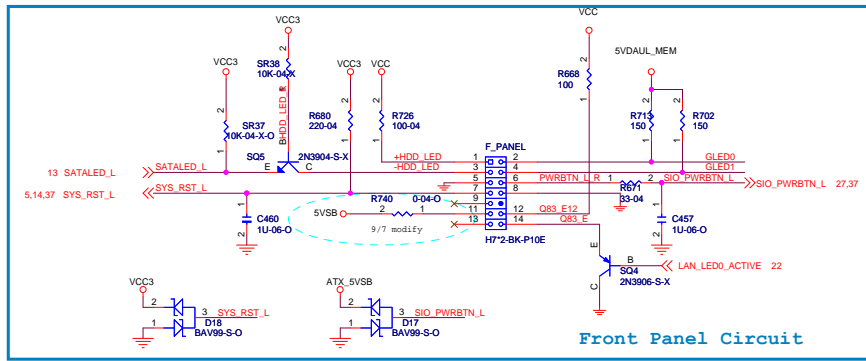
Date: Monday, December 20, 2010

Sheet: 26 of 45

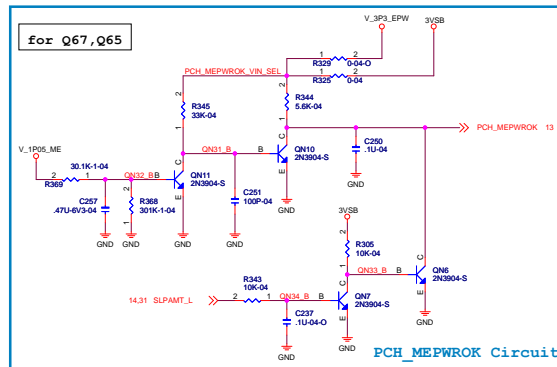
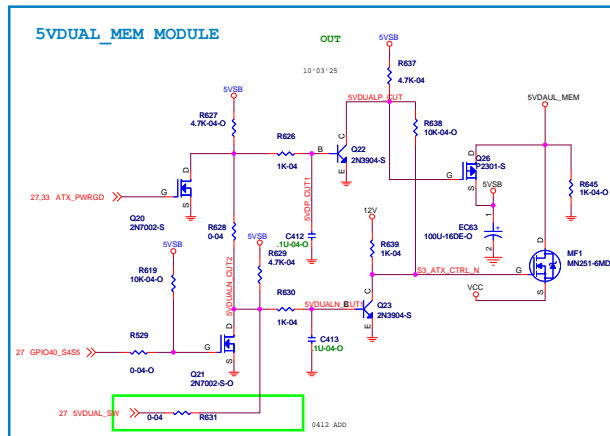
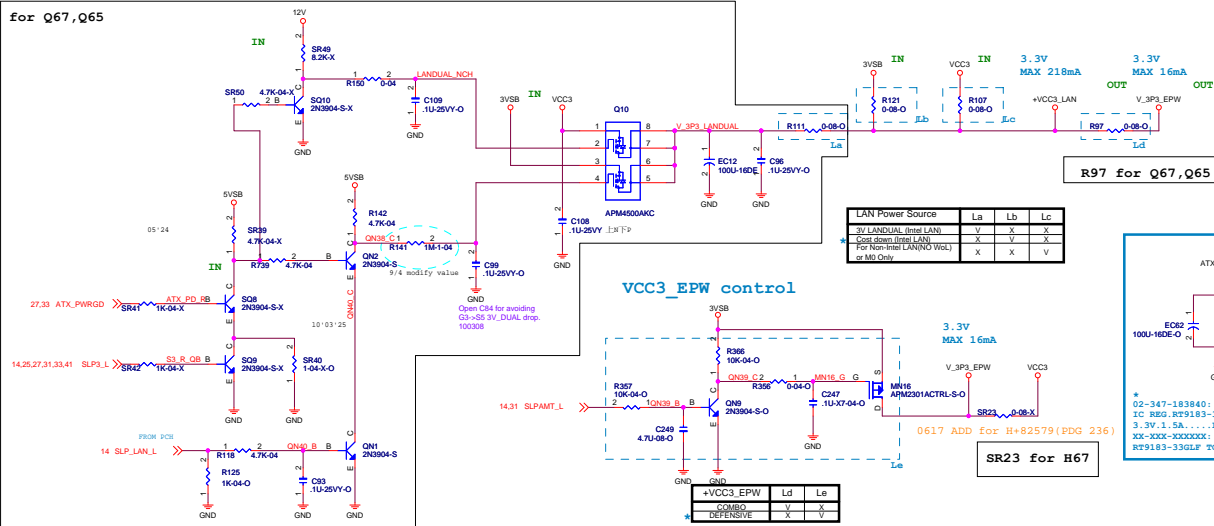
Rev: 1.0





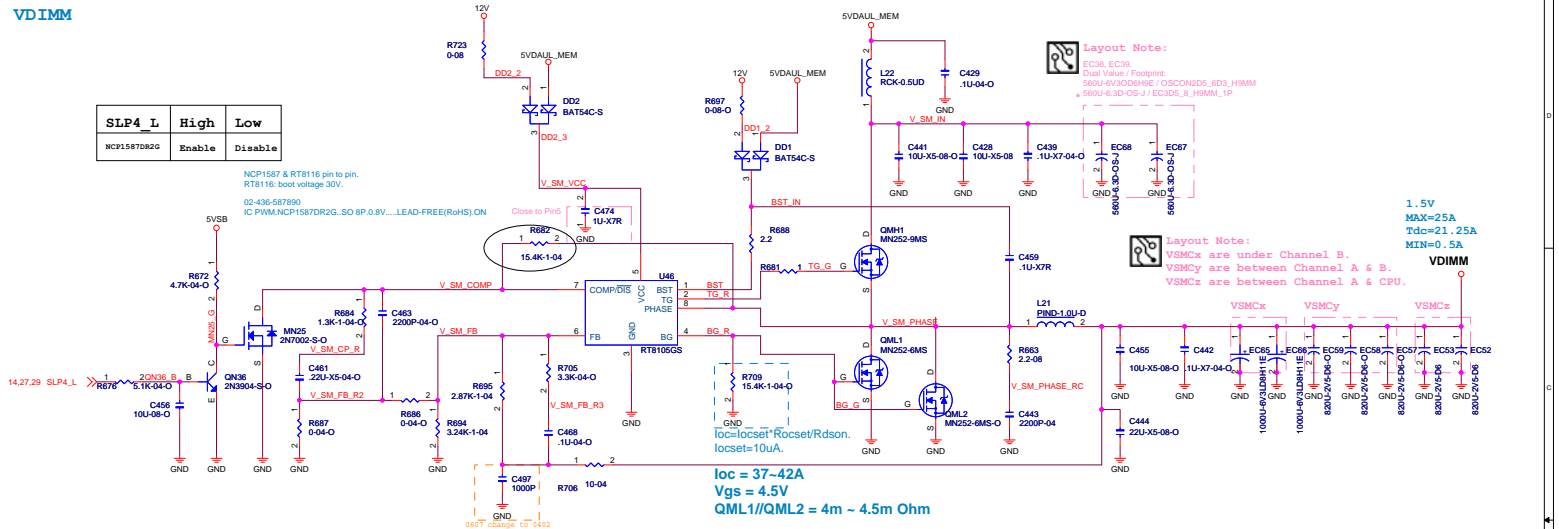


for Q67,Q65



SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.
Q2-436-587890
IC PWM.NCP1587DR2G.S0 8P 0.8V.....LEAD-FREE(RoHS)CN



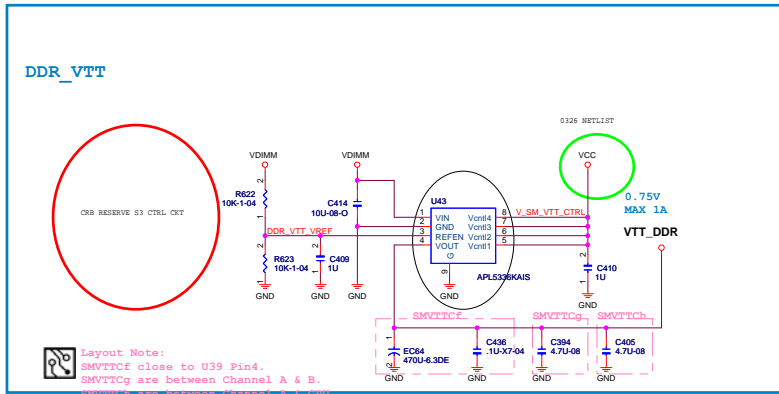
Layout Note:
EC38, EC39
Dual Value / Footprint:
580U-8V/300H1E / OSCNDS, RDS_HMM
+ 580U-4.3D-OS-1 / EC38, R_HMM_1P

Layout Note:
7.
VSMCx are under Channel B.
VSMCy are between Channel A & B.
VSMCz are between Channel A & CPU.

1.5V
MAX=25A
Tdc=21.25A
MIN=0.5A
VDIMM

loc = 37~42A
Vgs = 4.5V
QML1/QML2 = 4m ~ 4.5m Ohm

DDR_VTT



Layout Note:
SMVTTcF close to U39 Pin4.
SMVTTcG are between Channel A & B.
SMVTTcH are between Channel A & CPU.

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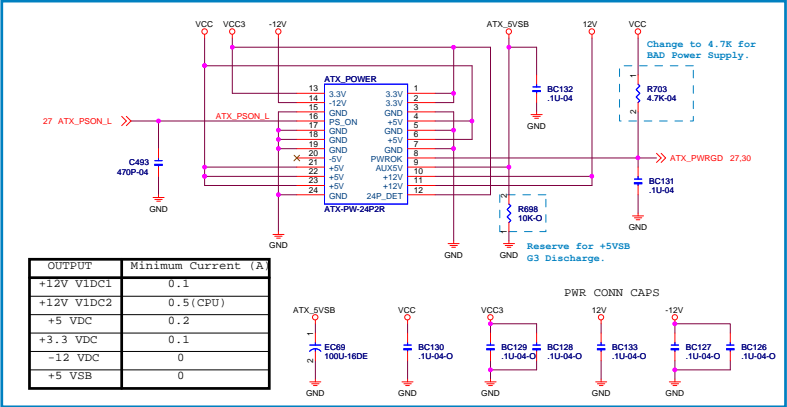
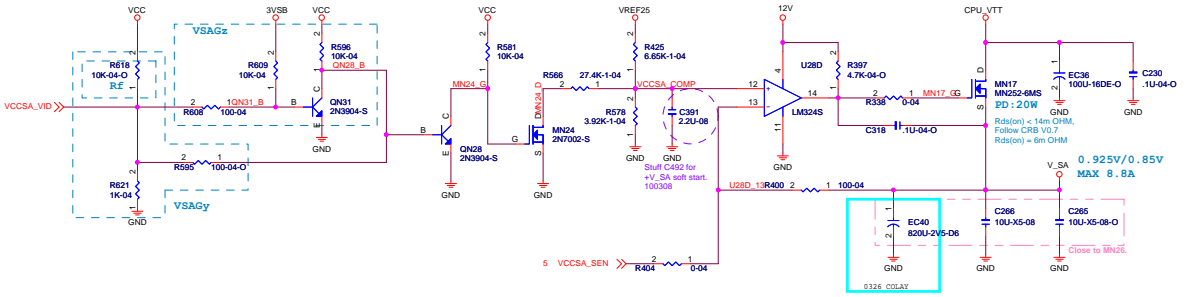
Title DC/DC VDIMM/DDR_VTT/5VDUAL		
Size	Document Number	Rev
Customer	H67H2-AM/Q67H2-AM/Q65H2-AM	1.0
Date	Monday, November 22, 2010	Sheet 32 of 45

Default Stuffed:

Stuff VSAGz	
VCCSA voltage selection	
VID	+V SA
0	0.925V
1	0.85V

Stuff VSAGy

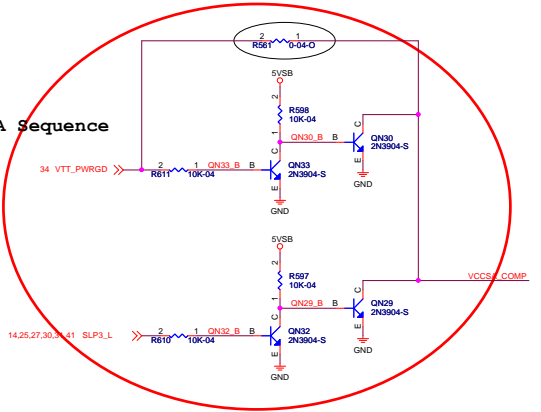
VCCSA voltage selection	
Rf	+V SA
unstuff	0.85V
stuff	0.925V



OUTPUT	Minimum Current (A)
+12V VIDC1	0.1
+12V VIDC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

ATX Power 24PIN

VCCSA Sequence



Title: DC/DC VCCSA, ATXPWR

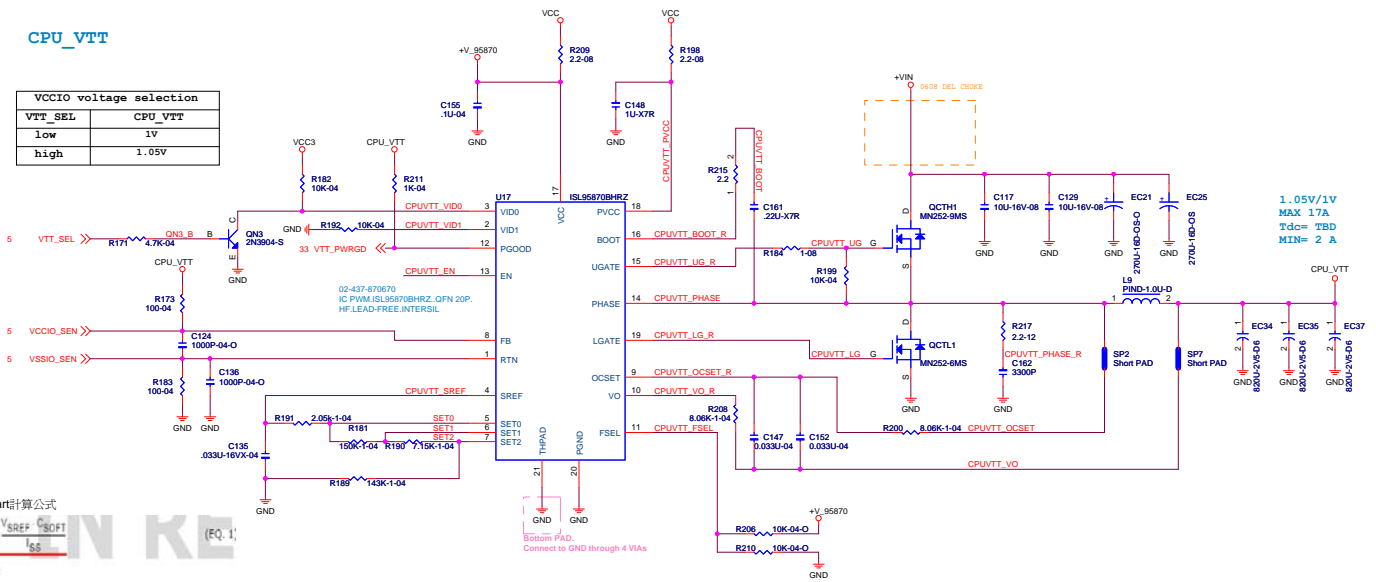
Size: Document Number: H67H2-AM/Q67H2-AM/Q65H2-AM

Customer: H67H2-AM/Q67H2-AM/Q65H2-AM

Date: Monday, November 22, 2010 Sheet 33 of 45

CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



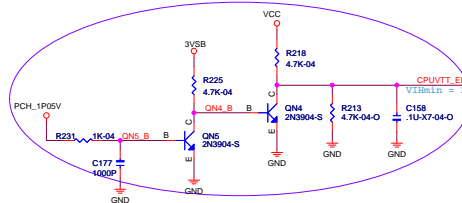
Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

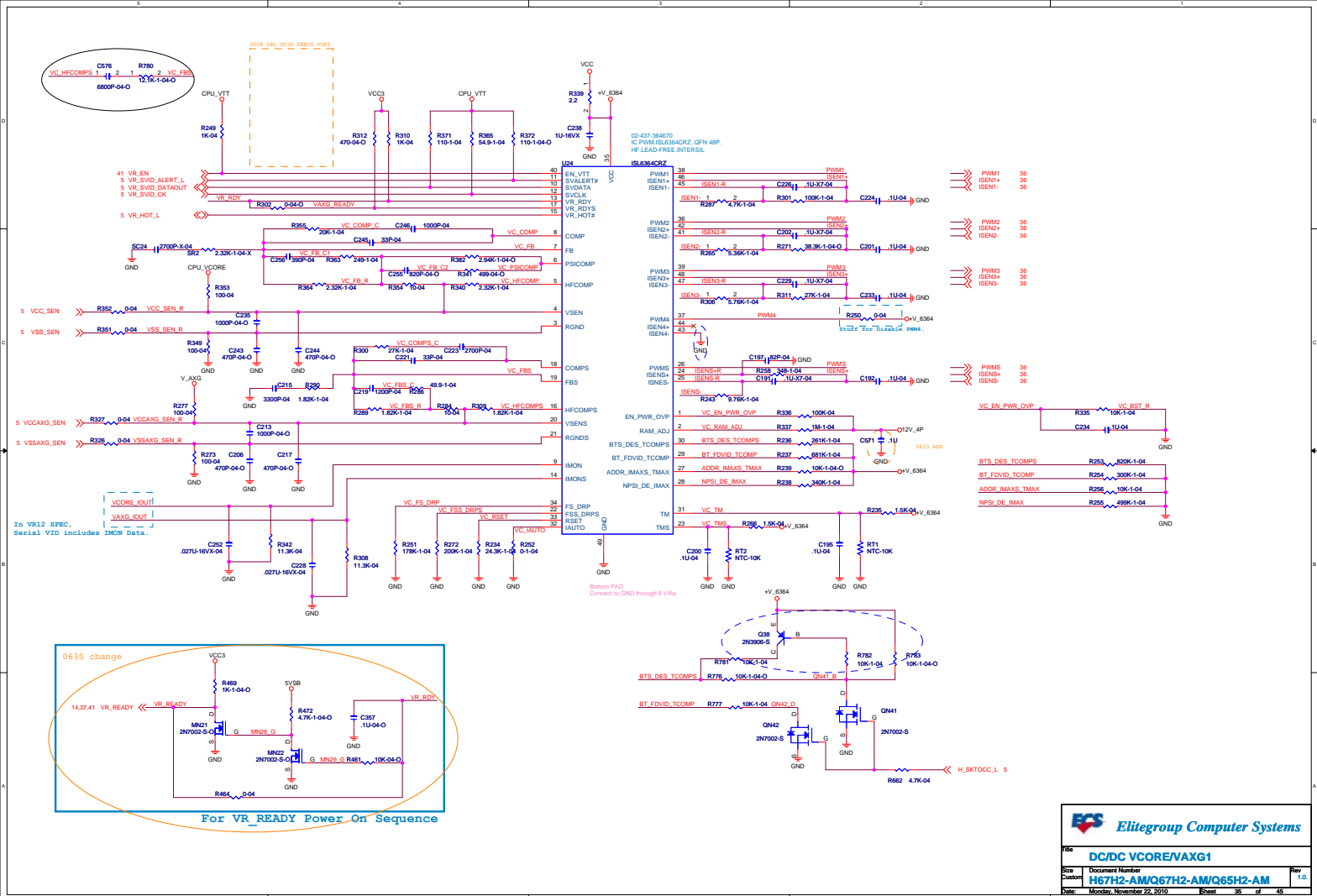
Vout計算公式

TABLE 2. ISL958700 VID TRUTH TABLE				
VID STATE		RESULT		
VID1	VID0	CLOSE	V _{REF}	V _{OUT}
1	1	SW0	V _{REF1}	V _{OUT1}
1	0	SW1	V _{REF2}	V _{OUT2}
0	1	SW2	V _{REF3}	V _{OUT3}
0	0	SW3	V _{REF4}	V _{OUT4}

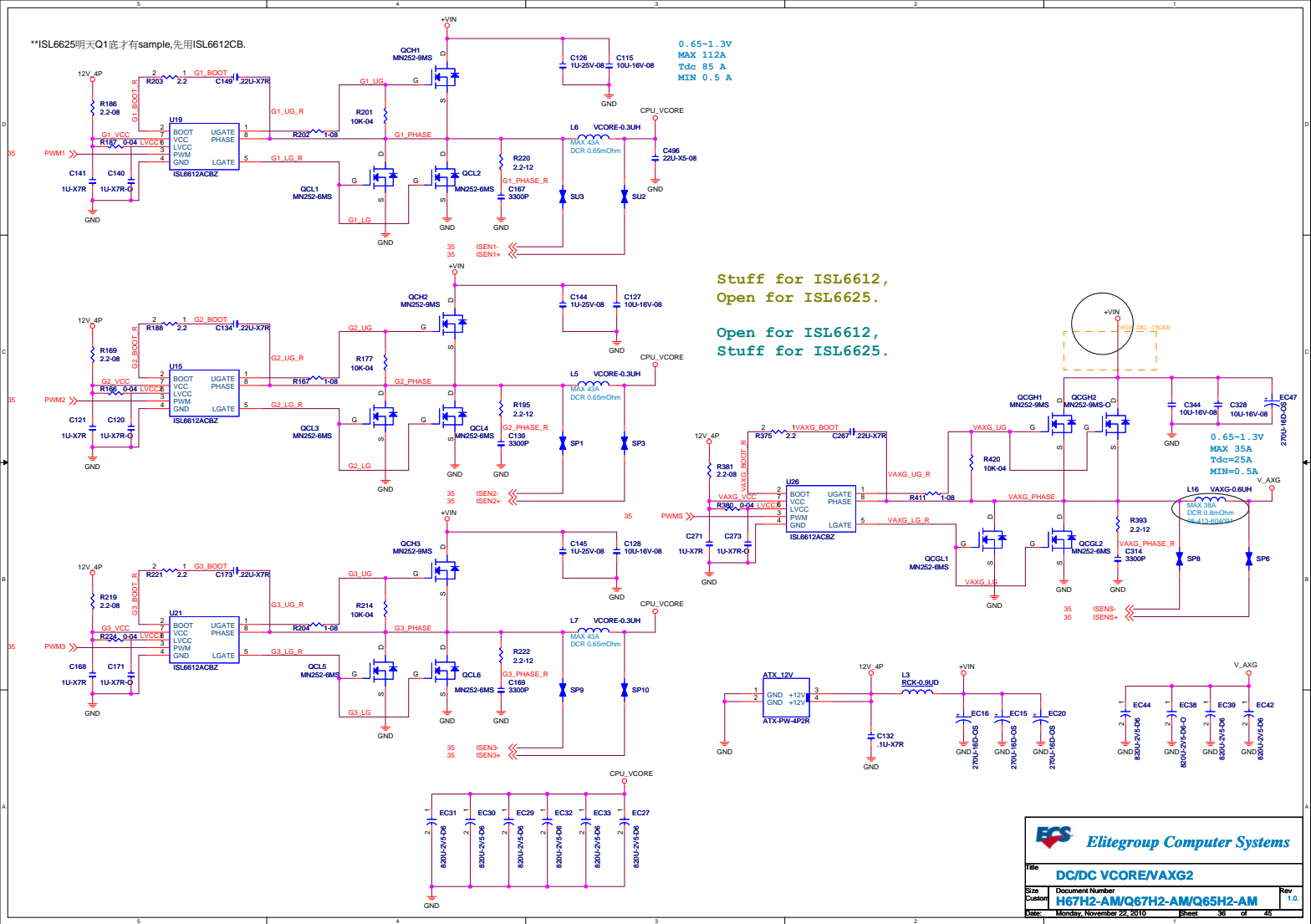
Equations 21, 22, 23 and 24 give the specific V_{REF} equations for the ISL958700 setpoint reference voltages:
 The ISL958700 V_{SET1} setpoint is written as Equation 21:
 $V_{SET1} = V_{REF}$ (EQ. 21)
 The ISL958700 V_{SET2} setpoint is written as Equation 22:
 $V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET4}}\right)$ (EQ. 22)
 The ISL958700 V_{SET3} setpoint is written as Equation 23:
 $V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right)$ (EQ. 23)
 The ISL958700 V_{SET4} setpoint is written as Equation 24:
 $V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right)$ (EQ. 24)

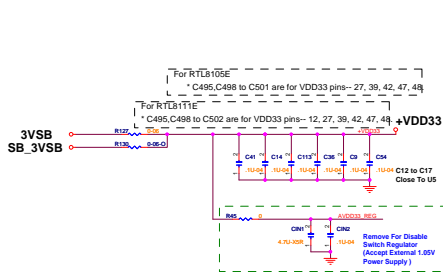
FIGURE 10. ISL958700 VOLTAGE PROGRAMMING CIRCUIT





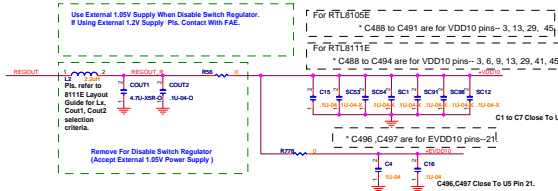
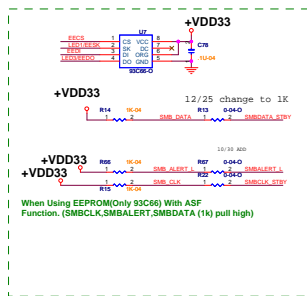
**ISL6625明天Q1底才有sample,先用ISL6612CB.



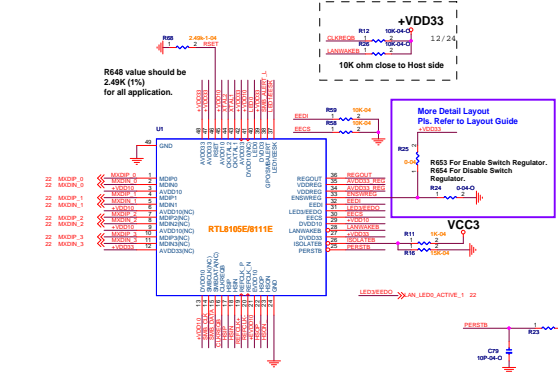


	L13	Cout1	Cout2	R645	R650
Enable Switch Regulator	O	O	O	O	O
Disable Switch Regulator	X	X	X	X	X

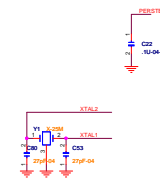
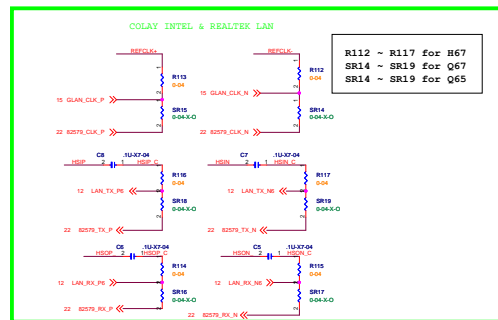
For RTL8111E EEPROM / ASF / Efuse Function (3 Option)



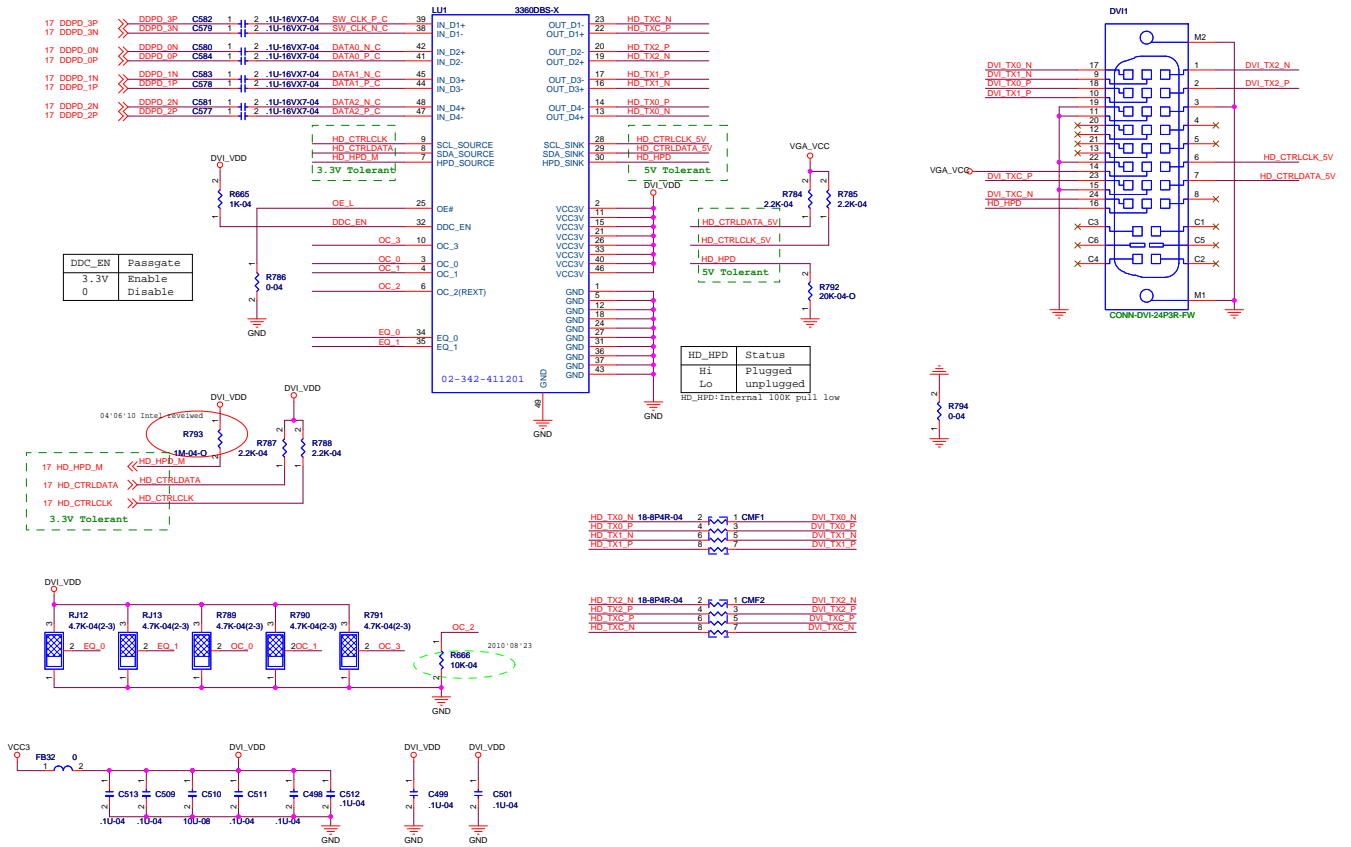
Controller

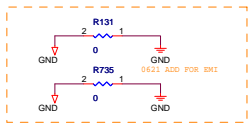
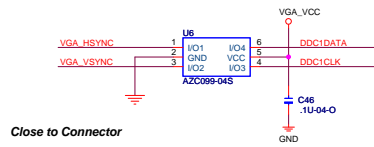
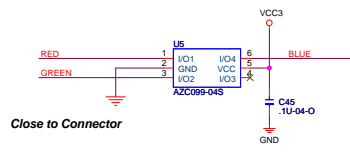
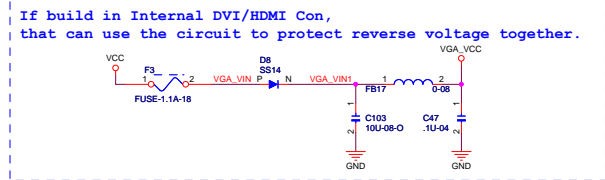
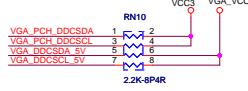
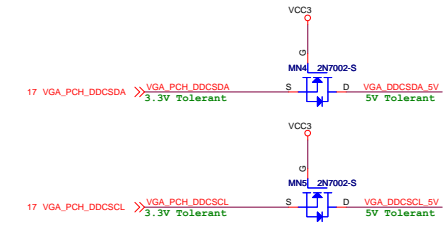
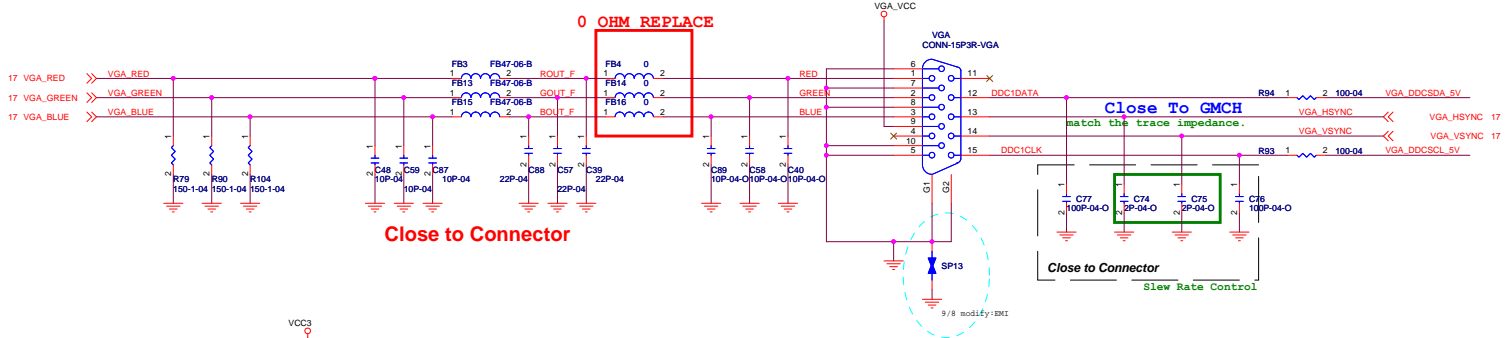


12/25 change LED control pin



Level Shifter





Elitegroup Computer Systems			
VGA CONNECTOR			
File	H67H2-AM/Q67H2-AM/Q65H2-AM		
Size	Custom	Document Number	Rev
H67H2-AM/Q67H2-AM/Q65H2-AM			1.0
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ATX P/S WITH 1A STBY CURRENT	ATX4P
5VSB +/-5%	5V +/-5%
3.3V +/-5%	3.3V +/-5%
12V +/-5%	12V +/-5%
-12V +/-5%	-12V +/-5%

Switching
ISL6364
4+1 phases

Vcore:0.65-1.3V 112Amax
Vaux:0.65-1.3V 35Amax

Switching
ISL958708
1 phase

V_CPG_VTT:1.05V 17Amax

Linear
LM324

VCC_SA:0.925V(0.85V) 8.8Amax

Switching
NCP1587

V_DIMM:1.5V 28.5Amax

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0 1.0A_S3
V_SM_VTT	1.0A_S0

DDR_VTT:0.75V

LDO
APL5336

Linear
LM324

PCR_CORE:1.05V 6.2Amax

Switching
RT8015A

V_MB:1.05V 1.8Amax

Linear
LM324

V_SPR:1.8V 1.6Amax

Non ART:
VccASW(MB) short to V1P05_PCH

Not support DSX mode:
VccDSW short to 3VSB

Intel Sandy Bridge CPU		
VCCP	V1D 0.25-1.52V	85A(80W)
VAXG	V1D 0.25-1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Cougar Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLLA	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.158A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.002A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.087A
VccSUSHDA	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
VSREF	5V	1mA
VSREF_SUS	5V	1mA

LAN INTEL 82579		
VDD3P3	3.3V	90mA
VDD1P0	1V	332mA
CTRL1P0 internal LVR Output		

SUPER I/O IT8723		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC662-VC		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery
3V

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

Total 1 Slot

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
Total 2 Slots	

Total 2 Slots

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)

Total 1 Slot

USB X4 Header
VDD
5VDual
2.0A

USB X4 IO
VDD
5VDual
2.0A

PS/2
Dual
A

3VSB

VCC3

VCC3

VCC3

5VSB

12V

LDO

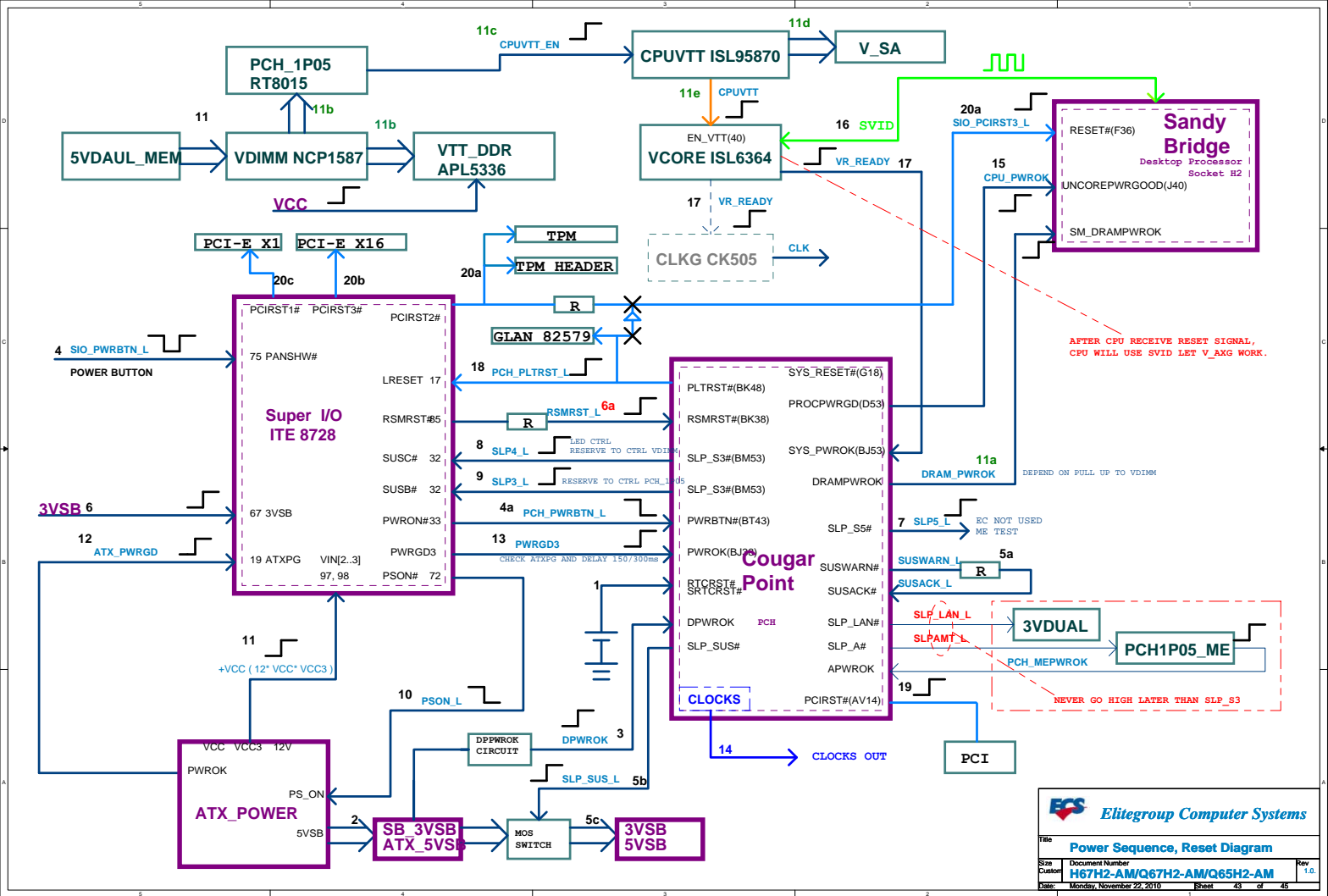
5V

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Power Delivery

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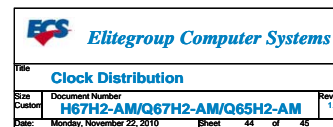


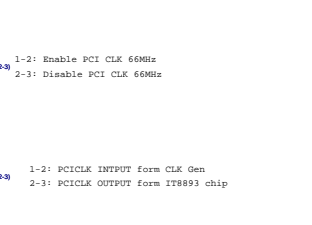
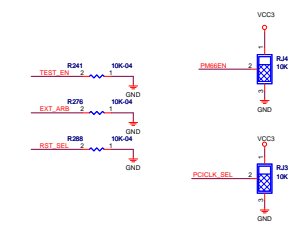
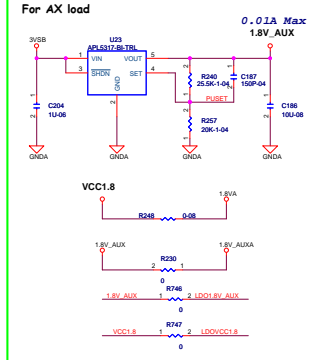
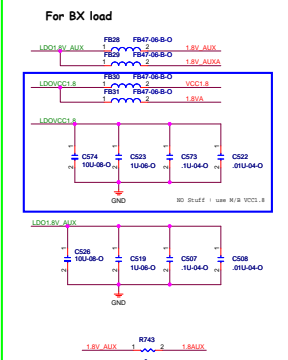
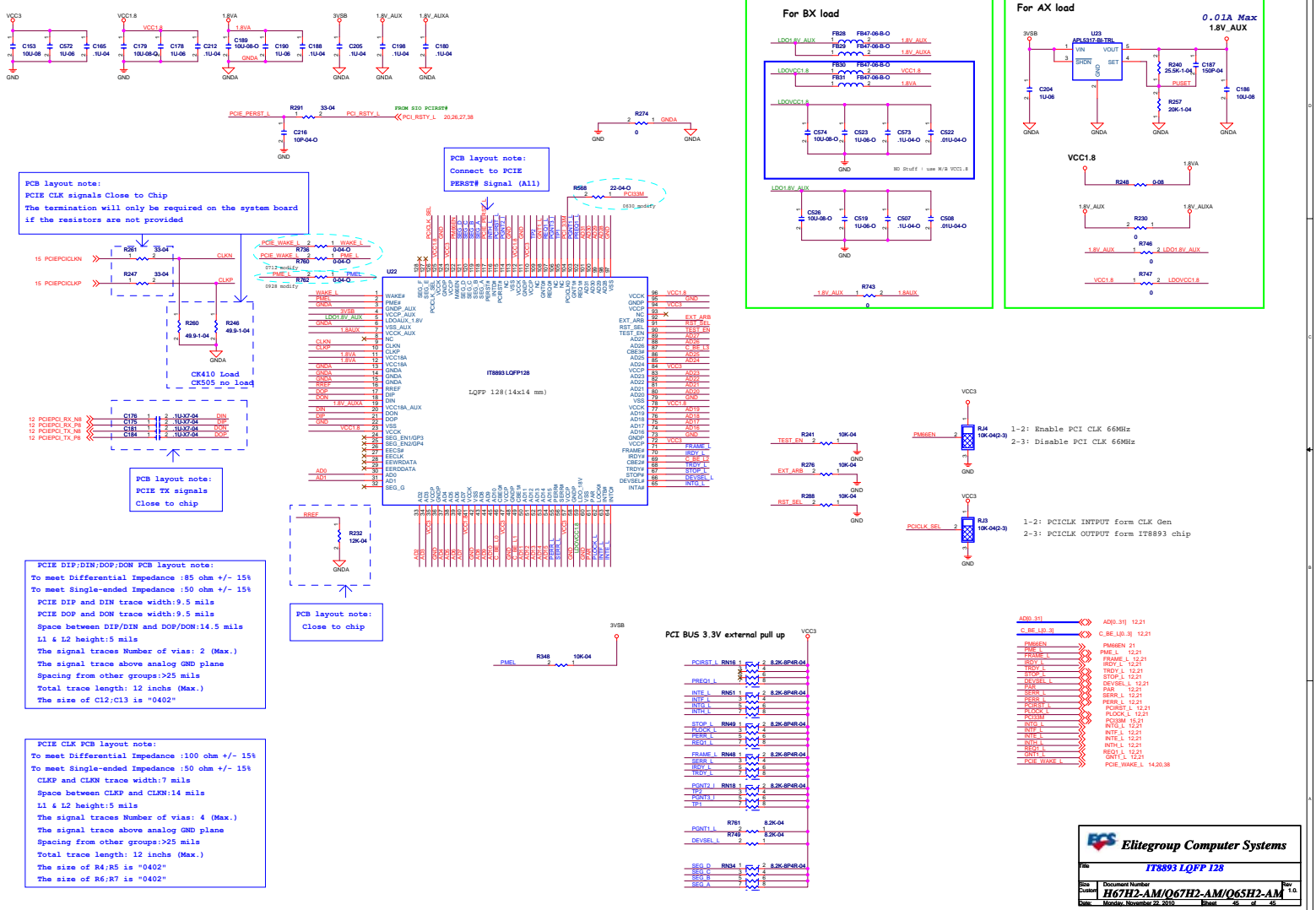
NOTE:

- 1. Sugar Bay Platform has two clock mode:
 - a. Integrated Clock Mode (Generate by PCH)
 - b. Buffer Through Mode (Generate by Clock Gen.)
- 2. If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

- Page.12 PCH - DMA/PCI/PE/USB for CLK IN PD
- Page.13 PCH - SATA, SATA CONN for CLK IN PD
- Page.14 PCH - MISC, F/W Strap
- Page.15 PCH - CLK IO, CKG





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I78893 LQFP 128

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